# Electronics
## From Theory into Practice

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# *Electronics – from Theory into Practice*

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BY

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AND

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# Contents

# Preface

To ALL students of electronics there comes a time when a specification is presented to them and they are expected to turn their theoretical knowledge into practice. Many find this is a difficult step to take. The aim of this book is, where possible, to formalize design procedures covering a wide range of electronic circuitry, and thus to bridge the gap between theory and practice. It is also hoped that the book will be of use to practising engineers, particularly those trained in other disciplines, who, due to the widespread application of industrial control and automation, are obliged to undertake a certain amount of electronic design.

The first two chapters introduce the reader to the thermionic valve and the transistor and show how data sheets, provided by the manufacturer, are used in design calculations. There follows eight chapters devoted to specific subjects. Each of these contain a brief treatment of theory limited to the extraction of necessary design relationships. Design procedures are established, followed by worked design examples to meet given specifications. The book is concluded with a chapter on general electronic engineering practice.

The authors wish to express their gratitude to Mrs. D. Swift and Miss D. Sargent for their assistance in the preparation of this book.

J. E. FISHER
H. B. GATLAND

*Cranfield*, 1966

# Design Examples

CHAPTER 1

# The Thermionic Valve

## Introduction

A thermionic valve is a device which utilizes the flow of electrons through a vacuum or near vacuum. Electrons are emitted by a heated cathode and collected by an anode which is generally held at a positive voltage with respect to the cathode. The introduction of other electrodes enables the stream of electrons from cathode to anode to be suitably controlled. The whole electrode assembly is usually mounted in a glass envelope from which all gas has been evacuated, although in some types, a trace of gas is intentionally introduced to modify the valve characteristics.[1]

## Functional Survey of Valve Types

### 1.1. The Diode

The diode is the simplest form of thermionic valve comprising a heated emitting cathode and a collector anode. It has largely been superseded by the semiconductor diode which, in its various forms, has lower forward resistance, better performance at h.f., no heater requirement, and a true zero.

The characteristic curve of a typical thermionic diode has the form shown in Fig. 1.1b. Anode current $I_A$ is plotted against anode voltage $V_A$, and an increase in heater voltage is seen to raise the value of $I_A$ at which saturation occurs. Because electrons leave the cathode with a finite velocity, some anode current flows when $V_A = 0$. This current increases with cathode

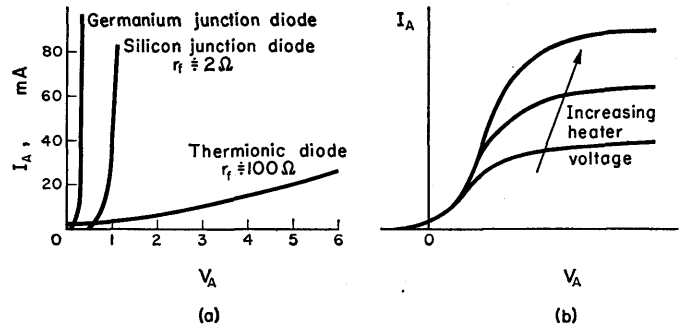



FIG. 1.1. (a) Comparison of thermionic and semiconductor diodes. (b) Effect of heater voltages on diode characteristics.

temperature giving a displacement of the characteristic to the left, of approximately 0·1 V per 10% change in heater voltage.

Below saturation, the Three-halves Power Law[2] holds, i.e.

$$I_A = kV_A^{3/2}, \tag{1.1}$$

where $k$ is a constant determined by the geometry of the valve.

*Applications.* Typical applications of the thermionic diode are illustrated in Fig. 1.2.

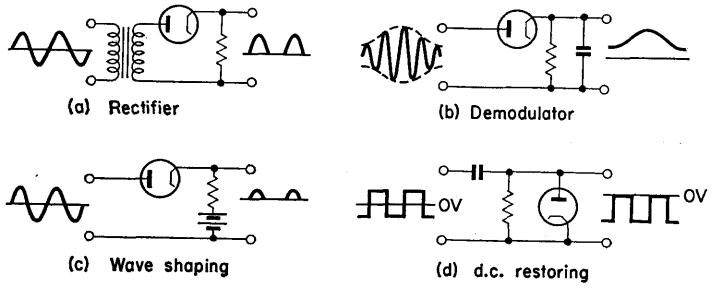



FIG. 1.2. Applications of the thermionic diode.

## 1.2. The Triode

A triode valve has three electrodes, a control grid being introduced between cathode and anode. The anode current is controlled by varying $V_{GK}$, the voltage between the grid and cathode. Small changes in $V_{GK}$ can cause large changes in $I_A$ with negligible expenditure of power in the grid circuit.

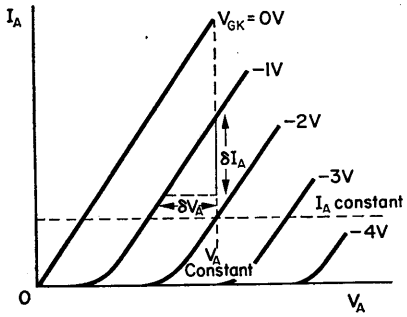



FIG. 1.3. Typical anode characteristics of a triode.

A typical family of anode characteristic curves is given in Fig. 1.3 in which $I_A$ is plotted against $V_A$ with $V_{GK}$ as parameter.

Using these curves, three fundamental relationships may be defined.

### (1) *Differential Anode Resistance*

The gradient of a curve at any point is

$$\left[\frac{\delta I_A}{\delta V_A}\right](V_G \text{ constant}) \underset{\text{def}}{=} g_a = \frac{1}{r_a}, \qquad (1.2)$$

where $r_a$ is the differential anode resistance.

(2) *Mutual Conductance*

Intercepts of lines parallel to the current axis give

$$\left[\frac{\delta I_A}{\delta V_G}\right](V_A \text{ constant}) \underset{\text{def}}{=} g_m, \tag{1.3}$$

where $g_m$ is the mutual conductance or transconductance.

(3) *Amplification Factor*

Intercepts of lines parallel to the voltage axis give

$$\left[\frac{\delta V_A}{\delta V_G}\right](I_A \text{ constant}) \underset{\text{def}}{=} \mu, \tag{1.4}$$

where $\mu$ is the amplification factor.

Expression (1.1), giving the anode current of a diode as a function of anode voltage, can be extended for the triode

$$I_A = K\left(V_G + \frac{V_A}{\mu}\right)^{3/2}. \tag{1.5}$$

Thus if $V_G$ is negative and $V_G = -V_A/\mu$, then $I_A = 0$. This value of grid voltage is the *grid cut-off voltage* $V_{Gc/o}$, and is a function of $\mu$ and anode voltage.

EXAMPLE. With an anode voltage of 180 V, a valve having $\mu = 50$ has a grid cut-off voltage,

$$V_{Gc/o} = -V_A/\mu = -180/50 = -3{\cdot}6 \text{ V}.$$

Since the cut-off voltage is inversely proportional to $\mu$, high $\mu$ valves have a smaller input handling capacity than low $\mu$ types for a given $V_A$. Usual operation is with the grid voltage in the range 0 V to $V_{Gc/o}$. If the grid is positive with respect to the cathode, it will attract electrons and grid current will flow. Under these conditions there is a low resistance between grid and cathode, of the order of 1000 Ω.

There are three general types of triode valves, typified by the 12AU7, 12AX7 and 12AT7, whose anode characteristics are given in Fig. 1.4.

(a) Low $\mu$, low $g_m$: 12AU7 with $\mu = 20$ and $g_m = 2$ mA/V.
(b) High $\mu$, low $g_m$: 12AX7 with $\mu = 100$ and $g_m = 2$ mA/V.
(c) Medium $\mu$, high $g_m$: 12AT7 with $\mu = 50$ and $g_m = 4$ mA/V.

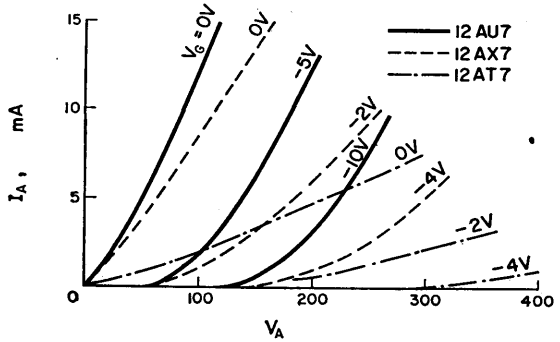



FIG. 1.4. Anode characteristics of 12AT7, 12AU7 and 12AX7 triodes.

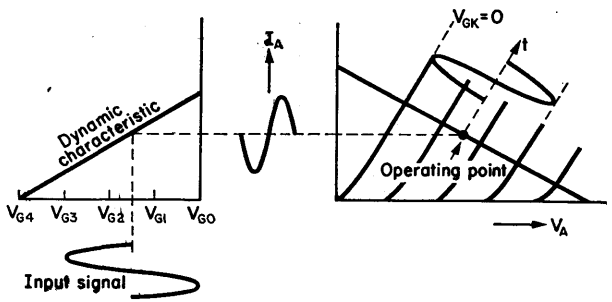



FIG. 1.5. The triode as a linear amplifier.

Suggested uses for these three groups are:

(a) *Low $\mu$.* Where large input signals are to be handled, such as in frequency multiplying tuned amplifier stages.

(b) *High* $g_m$. Cathode follower stage where the output resistance tends to $1/g_m$.

(c) *High* $\mu$. A voltage amplifier where the highest possible gain is required. For any common cathode amplifier the maximum gain is $\mu$.

The group of valves having high $g_m$ and medium $\mu$ is probably the more generally applicable type.

*Applications.* Amplifiers at low frequencies where interelectrode capacitance has only limited effect.

Tuned amplifiers at v.h.f. where the low noise performance of a triode makes it preferable to a pentode.[3]

Oscillators of both sinusoidal and relaxation types. In many cases two triodes are mounted in the same envelope. This is very convenient for pulse networks of the multivibrator type.

## 1.3. The Tetrode (Fig. 1.6)

The screen grid was introduced to enable h.f. amplification to be accomplished without the necessity of neutralizing the grid to anode capacitance (§ 1.5). However, secondary emission

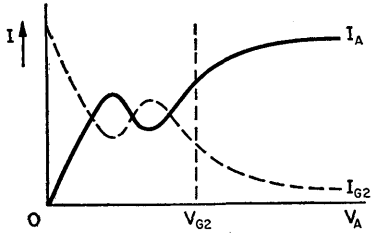



Fig. 1.6. Elementary tetrode characteristics, showing negative resistance region due to secondary emission.

effects,[2] when the anode is at a lower voltage than the screen grid, reduce the usefulness of the valve. This limitation led to the introduction of the suppressor grid in the pentode.

Beam tetrodes, in which the electron stream is directed in such a manner as to give a potential minimum between the

screen grid and anode, are widely used for low and medium power amplifiers. The screen current in these types is a very small part of the cathode current as the grids are aligned and the screen grid intercepts few electrons.

Since the screen current performs no useful work, in most cases it is desirable that it should be as small as possible.

*Applications.* In addition to their use as power amplifiers, tetrodes are also widely used as series regulator valves in stabilized power supplies.

## 1.4. The Pentode

The suppressor grid produces a potential minimum between the anode and screen grid which prevents secondary electrons, generated at the anode, from being collected by the screen grid. The suppressor is usually maintained at the cathode voltage, but it can be used as a control grid with respect to anode current. Generally, $V_{Gc/o}$ is of the order of $-50$ V, but special purpose pentodes have been developed with suppressor cut-off of only a few volts.

Examination of the typical pentode characteristics of Fig. 1.7 shows that beyond $V_A = 100$ V the curves are nearly parallel to

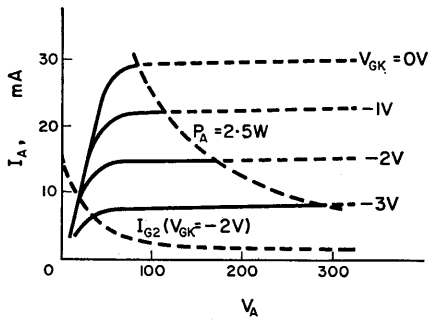



FIG. 1.7. Typical pentode characteristics. The broken line region of the curves shows where the maximum permissible anode dissipation is exceeded.

the voltage axis, indicating a large $r_a$ ($\doteqdot$ 1 MΩ). Thus, above the knee of the curves the anode current is largely independent of anode voltage. This is because the screen grid voltage controls the anode current by providing the accelerating electric field. Due to the passive nature of the anode, the $\mu$ for pentodes is extremely high, commonly being greater than 1000.

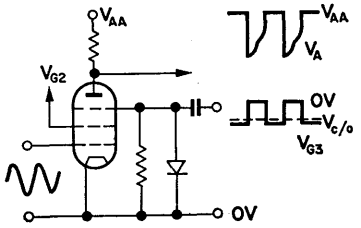



FIG. 1.8. Use of a pentode for gating purposes. The gating waveform is applied to the suppressor grid.

At low values of $V_A$ the curves run together. Thus, for a given load line the value of the minimum anode voltage is fixed. (This is not so for the triode.) The minimum anode voltage for a pentode is known as the *bottoming voltage* and is of importance in many "non-linear" operations. It should be noted that if $V_{G2}$ is fixed, the cathode current $I_A + I_S$ is constant for a given value of $V_{G1}$.

*Applications.* Pentodes are widely used as tuned amplifiers because, due to small anode–grid capacitance, stable operation can be achieved without neutralization. Much larger gain-bandwidth products are obtained with pentodes than with triodes, because of their low effective input capacitance. They are also used as voltage amplifiers for low frequency operation where large anode resistors can be used and the inherent high $\mu$ of the valves utilized. Very high gain can be obtained with low screen voltage giving the so-called "starvation condition". The circuit of Fig. 1.8 illustrates how the pentode may be used for gating purposes if the suppressor is used as a control grid. (See § 10.22.)

## 1.5. Grid Input Admittance

The interelectrode capacitances of a triode may be shown as in Fig. 1.9 in which $C_{ag}$ is the anode–grid capacitance and $C_{gk}$ the capacitance which exists between grid and cathode.

Input admittance $= i_{in}/v_{in} = (i_1 + i_2)/v_{in}$, where

$$i_{in} = v_{in}(1 - A)\, sC_{ag} \quad \text{and} \quad i_2 = v_{in} sC_{gk}.$$

Therefore

$$\text{Input admittance} = s(C_{gk} + (1 - A)\, C_{ag}). \qquad (1.6)$$

The symbol $s$ is the Laplace variable and where consideration is limited to sinusoidal operation this may be replaced by $j\omega$. Hence,

$$\text{Input admittance} = j\omega\, [C_{gk} + (1 - A)\, C_{ag}]. \qquad (1.7)$$

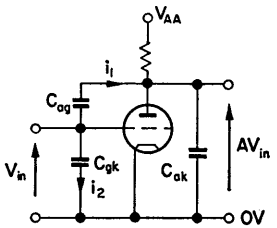



FIG. 1.9. Interelectrode capacitances of a triode.

The input capacitance is thus increased from $C_{gk}$ to

$$C_{gk} + (1 - A)\, C_{ag},$$

where $A$ is negative and greater than 1 at medium frequencies. This increase in effective input capacitance, due to the presence of anode–grid capacitance is the *Miller effect*,[4] and it was to reduce this effect that the screen grid was incorporated in the thermionic valve.

## 1.6. Auxiliary Voltage Supplies

### *Cathode Bias*

It is common practice to derive the auxiliary voltage supplies from the positive voltage rail which provides the anode supply. For a triode, a grid–cathode bias voltage is normally required to maintain the correct operating point, and cathode bias is used. This has two forms whose use depends on whether the amplifier is capacitor coupled or of the zero frequency type.

The cathode resistor $R_K$, in Fig. 1.10, in addition to providing the bias voltage, by negative current feedback, stabilizes the working point against variations such as ageing of the valve.

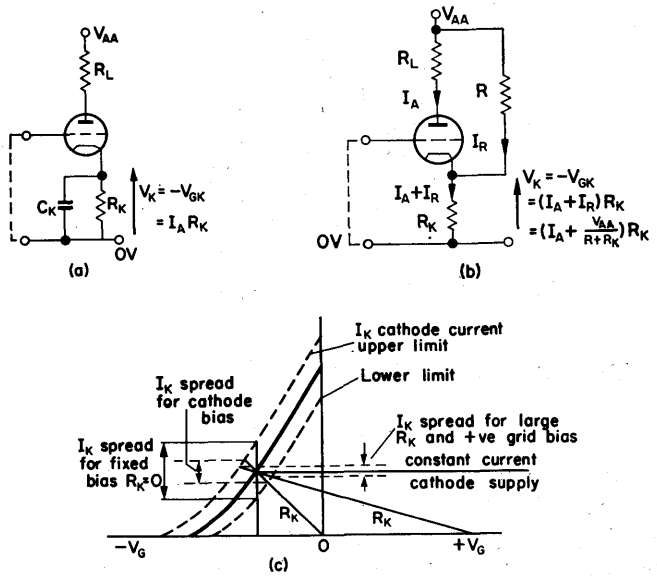



FIG. 1.10. Provision of cathode bias. The possible variation in operating point for cathode bias is less than for fixed grid bias, but is greater than for an ideal constant current supply. This latter can be approached by returning the grid to a positive supply.

To eliminate the negative feedback at signal frequencies and the consequent loss in gain, $R_K$ is bypassed by a capacitor of such value that in the required frequency range its reactance is negligible. (See § 3.6.)

If the loss in gain at zero frequency cannot be tolerated, the circuit of Fig. 1.10b may be used. Negative feedback is greatly

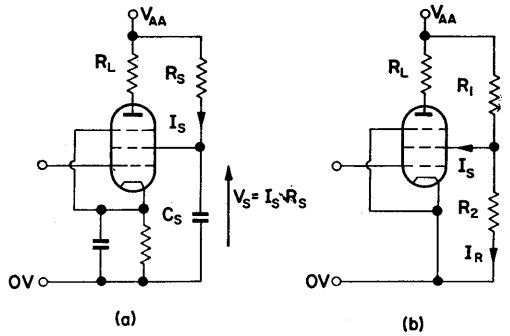



FIG. 1.11. Provision of screen grid supply from positive voltage rail, (a) current, (b) voltage.

reduced by making $R_K$ as small as possible, and the correct bias obtained by the steady current drawn through $R$. A typical value for $I_R$ is $10I_A$.

Then,

$$I_R = V_{AA}/(R + R_K) \doteqdot V_{AA}/R.$$

Also,

$$R_K = V_{GK}/(I_A + I_R) \doteqdot V_{GK}/I_R.$$

Therefore

$$V_K = -V_{GK} = (I_A + I_R)\, R_K = [I_A + V_{AA}/(R + R_K)]\, R_K.$$

## 1.7. SCREEN GRID SUPPLY

There are two commonly used methods of obtaining the screen grid supply from the positive voltage rail, (1) current and (2) voltage, as shown in Fig. 1.11a and b.

*Screen Current Supply*

If $V_S$ is the required screen voltage, the current at that voltage is determined either from the valve characteristic curves or experimentally. Then $R_S = (V_{AA} - V_S)/I_S$. To eliminate gain reduction the screen must be decoupled by the capacitor $C_S$. Negative feedback makes this method unsuitable for use in Zero Frequency Amplifiers.

*Screen Voltage Supply*

The voltage $V_S$ is kept relatively constant by making $I_R$ much greater than $I_S$, typically $I_R = 10I_S$. Then $R_2 = V_S/I_R$, and $R_1 = (V_{AA} - V_S)/(I_R + I_S)$. The disadvantage of this method is the drain on the h.t. power supply.

## 1.8. Elementary Valve Equivalent Networks

For input signals of small amplitude the valve parameters $g_m$, $\mu$ and $r_a$ can be considered as constants whose values are those measured at the operating point. Figure 1.12 shows how these parameters vary with $I_A$.

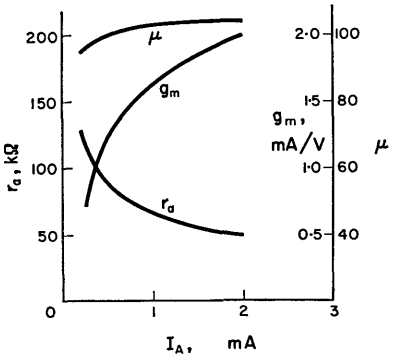



FIG. 1.12. Variation of $g_m$, $\mu$ and $r_a$, with $I_A$ as parameter, for an ECC85.

The anode current is a function of both grid voltage and anode voltage:

$$I_A = \frac{\delta I_A}{\delta V_G} \Delta V_G + \frac{\delta I_A}{\delta V_A} \Delta V_A. \tag{1.8}$$

If, for convenience, $\Delta I_A$ is written as $i_a$, an incremental change in anode current about the standing value $I_A$, and if $\Delta V_A$ is similarly represented as $v_a$, then

$$i_a = g_m v_g + g_a v_a. \tag{1.9}$$

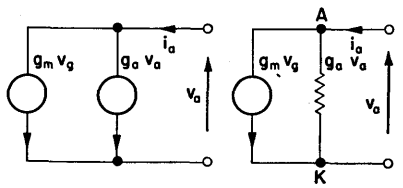



FIG. 1.13. Diagrammatic representation of eqn. (1.9) ($i_a = g_m v_g + g_a v_a$), using current generators.

This may be represented diagrammatically in the forms of Fig. 1.13.

Introducing an anode load resistor $R_L$ as in Fig. 1.14a, the equivalent network may be further developed as in Fig. 1.14b.

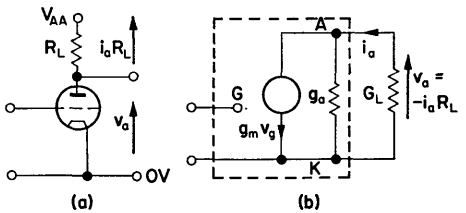



FIG. 1.14. Triode with anode load and its equivalent network.

As the anode voltage $v_a$ is a function of anode current, i.e. $v_a = -i_a R_L$, eqn. (1.9) may be written thus:

$$i_a = g_m v_g - i_a R_L / r_a.$$

Therefore

$$i_a r_a = g_m v_g r_a - i_a R_L.$$

But,

$$\mu = g_m \cdot r_a, \tag{1.10}$$

therefore

$$i_a = \frac{\mu v_g}{r_a + R_L}.$$

This expression provides the alternative equivalent network of Fig. 1.15.

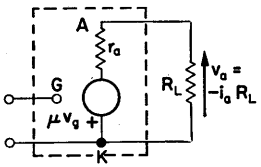



FIG. 1.15. Alternative equivalent network of the circuit of Fig. 1.14, using a voltage generator.

The voltage gain of the circuit may be written in the two forms as represented in the two equivalent networks. Thus:

$$v_a/v_g = -g_m/(g_a + G_L) = -g_m R, \tag{1.11a}$$

where

$$R = 1/(g_a + G_L),$$

and

$$\frac{v_a}{v_g} = \frac{-\mu R_L}{r_a + R_L}. \tag{1.11b}$$

A valve used in this way is said to be in *common cathode operation.*

## 1.9. RESISTANCE IN THE CATHODE

The circuit equations of Fig. 1.16 are

$$i_a = \frac{\mu v_{gk}}{r_a + R_L + R_K} \quad \text{and} \quad v_{gk} = v_{in} - i_a R_K.$$

Therefore

$$i_a = \frac{\mu v_{in}}{r_a + R_L + (\mu + 1) R_K} = \frac{\mu v_{in}}{r'_a + R_L}, \qquad (1.12)$$

where

$$r'_a = r_a + (\mu + 1) R_K.$$

The effective value of anode resistance is thus increased by the term $(\mu + 1) R_K$, and the equivalent network redrawn as in Fig. 1.17.

EXAMPLE. Given a valve having an anode resistance $r_a = 10\,\text{k}\Omega$ and gain $\mu = 50$, let $R_K = 1\,\text{k}\Omega$, and $R_L = 10\,\text{k}\Omega$. $r'_a = r_a + (\mu + 1) R_K = 10\,\text{k}\Omega + 51\,\text{k}\Omega = 61\,\text{k}\Omega$.

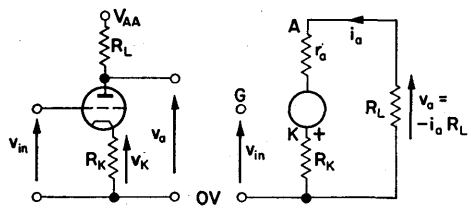



FIG. 1.16. Effect of cathode resistor.

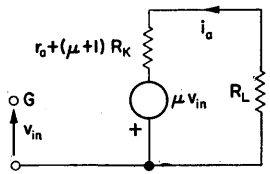



FIG. 1.17. Alternative equivalent network of the circuit of Fig. 1.16. $R_K$ is multiplied by $(\mu + 1)$ and transferred to the anode circuit.

In the absence of a cathode resistor, the voltage gain would be

$$A_v = -\mu R_L/(r_a + R_L) = -25.$$

This is modified by the cathode resistor thus:

$$A_v = -\mu R_L/(r'_a + R_L) = -7.$$

In the presence of both anode and cathode resistors, cathode voltage,

$$v_k = i_a R_K = \frac{\mu R_K}{r_a + R_L + (\mu + 1) R_K} v_{in}. \qquad (1.13)$$

$$\frac{\mu R_K/(\mu + 1)}{[(r_a + R_L)/(\mu + 1)] + R_K} v_{in} = \frac{\mu'' R_K}{r_a'' + R_K} v_{in}, \qquad (1.14)$$

where

$$\mu'' = \frac{\mu}{\mu + 1} \quad \text{and} \quad r_a'' = \frac{r_a + R_L}{\mu + 1}.$$

EXAMPLE. Using the same values as in the previous example,

$$\mu'' = 50/51 = 0{\cdot}98, \quad r_a'' = 20\,\text{k}\Omega/51 = 390\,\Omega,$$

and using expression (1.14),

$$\frac{v_k}{v_{in}} = \frac{0{\cdot}98 \times 1\,\text{k}\Omega}{390 + 1\,\text{k}\Omega} = 0{\cdot}7.$$

In the special case when $R_L = 0$, the valve is operated as a *cathode follower.*

Then,

$$\text{gain} = \frac{v_k}{v_{in}} = \frac{\mu R_K/(\mu + 1)}{[r_a/(\mu + 1)] + R_K} = 0{\cdot}81. \qquad (1.15)$$

The gain of a cathode follower tends to unity if $R_K$ is much greater than $r_a/(\mu + 1)$, and $\mu$ is much greater than 1.

The output resistance $r_a'' = r_a/(\mu + 1) \doteqdot 192\,\Omega$.

The output resistance of a cathode follower tends to $1/g_m$ if $\mu$ is much greater than 1.

The cathode follower is widely used as an impedance converter providing low output impedance from a high impedance source.

## 1.10. Signal injected at Cathode

The circuit of Fig. 1.18 is that or a common of "grounded grid" amplifier:

$$i_a = \frac{\mu v_{gk} - v_{in}}{r_a + R_L} \quad \text{and} \quad v_{gk} = v_{in}.$$

Therefore

$$i_a = \frac{-(\mu + 1)\, v_{in}}{r_a + R_L}, \tag{1.16}$$

and

$$v_a = \frac{(\mu + 1)\, v_{in} R_L}{r_a + R_L}. \tag{1.17}$$

This is similar to eqn. (1.11) except that $\mu$ has been replaced by $(\mu + 1)$. The main difference between common cathode and

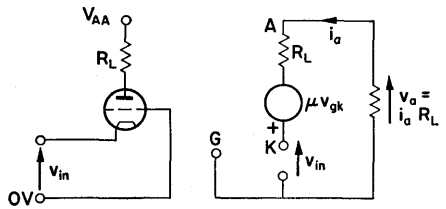



FIG. 1.18. Grounded grid amplifier. The input resistance is $(r_a + R_L)/(\mu + 1)$ because the anode current flows through the input circuit. No signal inversion occurs.

common grid operation is the resistance which the valve presents to the input signal source. In the common cathode case this is ideally infinite. The input resistance of a common grid amplifier, however, is

$$R_{in} = \frac{v_{in}}{i_a} \quad \text{(since the anode current flows through the input circuit)} \tag{1.18}$$

$$= v_{in} \times \frac{r_a + R_L}{(\mu + 1)\, v_{in}} = \frac{r_a + R_L}{(\mu + 1)}.$$

This normally has a value of a few hundred ohms, which means that the amplifier must be fed from a low resistance source such as a cathode follower.

## 1.11. Design from Characteristics

### *The Load Line*

For a given resistive load a line can be drawn on the anode characteristic giving the locus of points representing the anode voltage and current corresponding to the grid-to-cathode voltage. This line, the load line, has slope $-1/R_L$ (Fig. 1.19).

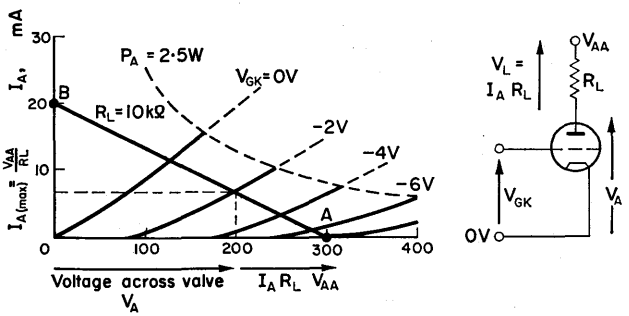



FIG. 1.19. Load line relationships, $R_L = 15\,\text{k}\Omega$, $V_{AA} = 300$ V, operating grid bias $= -2$ V.

Points $A$ and $B$ are the limits of the locus. When the valve is "cut off" the anode current is zero and the anode voltage is the supply voltage, that is, point $A$ on the characteristics ($V_A = V_{AA}$, $I_A = 0$). Point $B$ is found by determining the current that would flow if the voltage across the valve was zero, that is $I_{A(\max)} = V_{AA}/R_L$.

The equation of the load line is thus:

$$I_A = -G_L V_A + I_{A(\max)}. \tag{1.19}$$

For normal linear operation a point on the load line is chosen as operating point so that equal excursions in grid voltage about

that point give equal intervals on the load line, as shown in Fig. 1.5.

*Modification for Cathode Bias*

In the presence of a cathode resistor some modification of Fig. 1.19 is necessary. Let the cathode resistor be used to provide a bias of 2 V, then, at a standing anode current of $I_A = 6{\cdot}4$ mA,

$$R_K = -V_{GK}/I_A = 310\,\Omega.$$

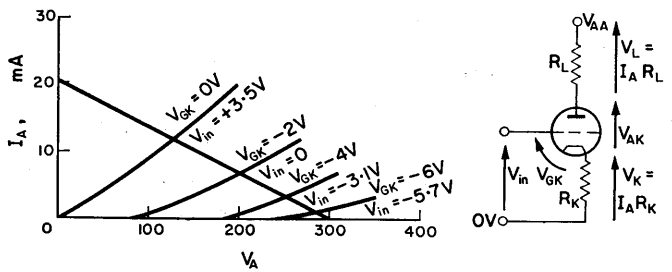



FIG. 1.20. Effect of cathode bias resistor. Note the increased range of input voltage.

This is negligible compared with $R_L = 15\,\text{k}\Omega$ and the load line is unchanged. However, the voltage $V_{GK}$ on the characteristics is no longer the input voltage, since

$$V_{in} = V_{GK} + I_A R_K. \tag{1.20}$$

Using this expression Table 1.1 can be constructed, and Fig. 1.19 redrawn as in Fig. 1.20.

It is apparent that the gain has been reduced and that the voltage handling capacity of the valve increased from 6 to 9 V. It is now also possible for the input voltage to go positive without the valve drawing grid current. In a.c. amplifiers the cathode resistor is normally bypassed with a large capacitor, and at the operating frequencies this effect of $R_K$ is eliminated.

TABLE 1.1

| $V_{GK}$ | $I_A$ (mA) | $V_K = I_A R_K$ | $V_{in} = V_{GK} + I_A R_K$ |
|---|---|---|---|
| 0 | 11·4 | 3·5 | 3·5 |
| −2 | 6·4 | 2·0 | 0 |
| −4 | 3·0 | 0·93 | −3·1 |
| −6 | 0·9 | 0·28 | −5·7 |

*Valve with Large Cathode Resistor*

If $R_K$ is large it is necessary to plot a load line having the value $R_L + R_K$, and, as previously, consider the circuit as having an input voltage $V_{in} = V_{GK} + I_A R_L$.

EXAMPLE. The symmetrical cathode coupled amplifier of Fig. 1.21. The anode voltages can be determined by considering

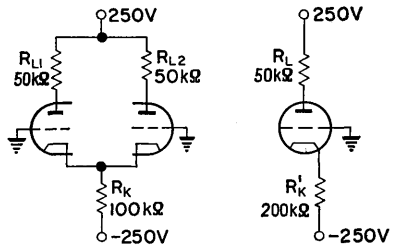



FIG. 1.21. Symmetrical cathode coupled amplifier with an equivalent single valve circuit for the balanced condition.

one valve. Since the anode currents of both valves pass through $R_K$, the cathode voltage is $V_K = 2I_A R_K = I_A \times 2R_K$, i.e. as if the anode current of one valve passes through a cathode resistor equal to $2R_K$. A load line must therefore be drawn having a value $R_L + 2R_K$ as in Fig. 1.22. The approximate d.c. conditions can be found in the following way. With the grids earthed the voltage between the negative rail and grid, $V_{in} = 250$ V. If the valves are to work in a linear manner the voltage dropped across $R_K$ must be within a few volts of that between the negative rail

and the grid, i.e. 250 V. The cathode current is thus determined by the value of the cathode resistor.

$$I_K = V_K/R_K = 250/100\ \text{k}\Omega = 2{\cdot}5\ \text{mA}.$$

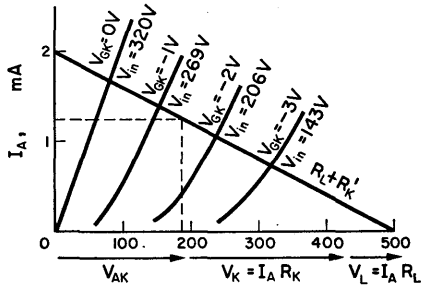



FIG. 1.22. Load line for $R_L + 2R_K$.

This current is shared between the two valves

$$I_{A1} = I_{A2} = 1{\cdot}25\ \text{mA}$$

in the balanced condition.

$$V_{A1} = V_{A2} = V_{AA} - I_A R_L = 250 - (1{\cdot}25 \times 50\ \text{k}\Omega) = 187{\cdot}5\ \text{V}.$$

From the load line $V_{GK} = -1{\cdot}3$ V.

This method of determining the approximate d.c. conditions can often be used with cathode coupled circuits.

*Cathode Follower*

In Fig. 1.23 the load line for $R_K = 10\ \text{k}\Omega$ is set up on the characteristic curves

$$V_{\text{in}} = V_{GK} + V_K = I_A R_K,$$

where $V_K$ is the output voltage $V_{\text{out}}$. From the load line the $V_{\text{out}}/V_{\text{in}}$ curve of Fig. 1.24 can be constructed.

When the input voltage $V_{\text{in}} = 0$ the output voltage equals $V_{\text{out}} = -V_{GK} = 6{\cdot}5$ V from the load line. When the cathode resistor is reduced, the voltage that the cathode follower can use

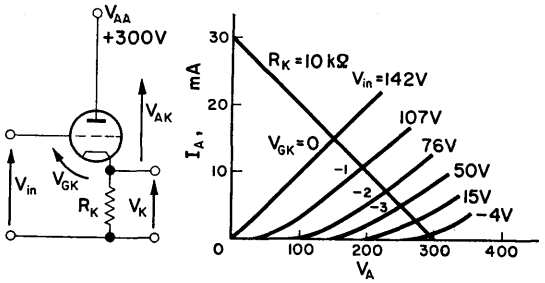



FIG. 1.23. The cathode follower. A load line for $R_K = 10\ k\Omega$ is plotted on the characteristic curves, together with the equivalent input voltages.

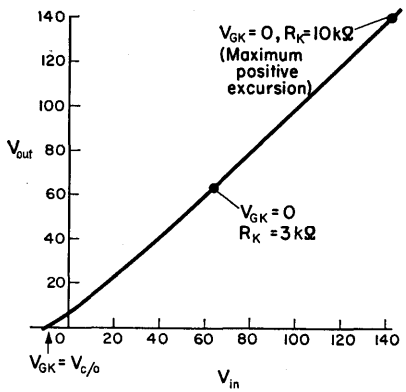



FIG. 1.24. $V_{out}/V_{in}$ curve for the cathode follower. Note that an increase in the value of $R_K$ increases the signal handling ability without changing the gain from unity.

over its linear range is reduced, but the input/output voltage relationship is little changed. The output voltage is a linear function of the input voltage and largely independent of the output current.

CHAPTER 2

# The Semiconductor

## Introduction

A semiconductor material is one having a specific resistance intermediate between that of an insulator and a conductor, the value of which decreases rapidly with rising temperature. Considering the atomic structure of such material, if sufficient energy is provided, by heating for instance, electrons will be released from their nuclei, each leaving behind it a hole. Under the influence of an electric field, an electric current will flow, which may be regarded as a movement of electrons in one direction and a movement of holes in the opposite direction. In the case of a pure or intrinsic semiconductor the numbers of holes and free electrons are always equal. The two materials commonly in use are germanium and silicon, both of which come from chemical Group IV.

If a semiconductor is doped with an element from Group V, say arsenic, the equality of free electrons and holes will no longer exist, there being an excess of free electrons. An electric current through such a material will then consist mostly of a flow of electrons in one direction and relatively few holes moving in the opposite direction. In this case the electrons are called *majority carriers* and the holes, *minority carriers.* A semiconductor doped in this way is known as *n* type material since the majority carriers possess negative charge.

A similar state of affairs will occur if the semiconductor is doped with an element such as indium from Group III. However, in this case an excess of holes will exist and these are the

majority carriers. Since the majority carrier possesses positive charge such a material is known as *p* type.

## 2.1. The Junction Diode[5]

If a piece of semiconductor material is doped with *p* type impurity at one end and *n* type impurity at the other, then there will exist a junction between the two types. Some holes in the *p* region will diffuse into the *n* region leaving the *p* region slightly

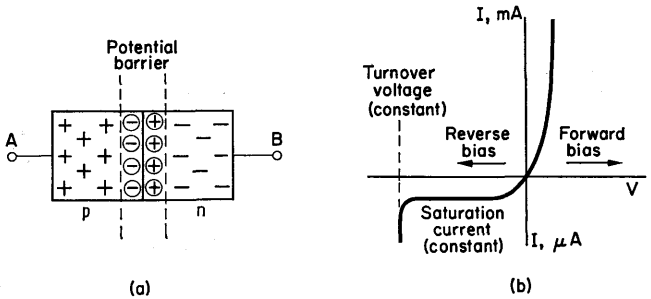



FIG. 2.1. (a) Semiconductor junction showing the potential barrier caused by the diffusion of charge carriers. Under these conditions a potential exists between *A* and *B*. (b) Characteristic curve of a semiconductor diode. Note the change in current scale as the curve passes through the origin.

negative. Similarly, electrons from the *n* region will diffuse into the *p* region causing it to become even more negative and leaving the *n* region slightly positive. Due to this diffusion the junction assumes a condition of dynamic equilibrium and acts as a potential barrier which opposes any further diffusion of charge. The condition is illustrated in Fig. 2.1a.

If bias is applied to the terminals such that *A* is positive with respect to *B*, it has the effect of reducing the potential barrier, and current will flow. This current increases exponentially with increasing voltage until the potential barrier is reduced to zero, when it is limited only by the resistance of the semiconductor material. If the bias is now reversed, the potential barrier is

increased and the majority carrier is blocked. There is, however, a finite current which flows, called the reverse saturation current. As the reverse bias is increased this current remains constant until the turnover point is reached, when the current increases rapidly at constant voltage (Fig. 2.1 b).

Thus, if a junction is biased in the forward direction, a fairly large current will flow, but under reverse bias conditions, provided the turnover voltage is not reached, the current is extremely small. In other words the device acts as a rectifier.

## 2.2. Leakage Current

This current varies from 1 to 200 μA for small germanium units, while silicon units have values much less than this. In both cases the current is dependent on temperature as is shown in Fig. 2.2 for a transistor with open circuit emitter.

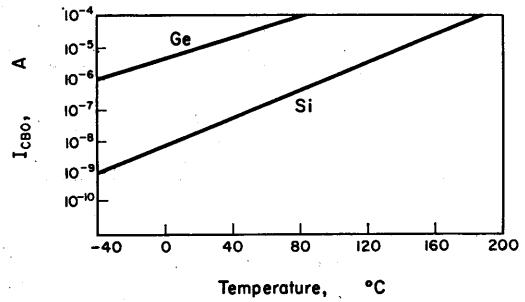



FIG. 2.2. Relationship between reverse saturation current and temperature for germanium and silicon.

The main causes of leakage current are:

(a) Minority carriers generated thermally, radiation effects and crystal imperfections. In these cases hole–electron pairs are formed and the charge carrier, which is the minority carrier, travels across the junction which is biased against the majority carrier. Generally, thermal generation is the more significant cause and the reverse saturation

current will increase by 10% for 1 °C rise (or doubles for an 8 °C rise). Because of this, the use of germanium devices is restricted to temperatures below about 70 °C. Silicon, however, is usable up to 150 °C.

(b) Surface leakage. This is a significant factor with silicon devices as the thermal current is very small within the unit itself, and surface paths, often caused by contamination, reduce the reverse resistance.

## 2.3. The Junction Transistor[6]

A typical alloy type junction transistor is illustrated in Fig. 2.3a and consists of a sandwich of doped semiconductor material, the base being more lightly doped than the collector and emitter,

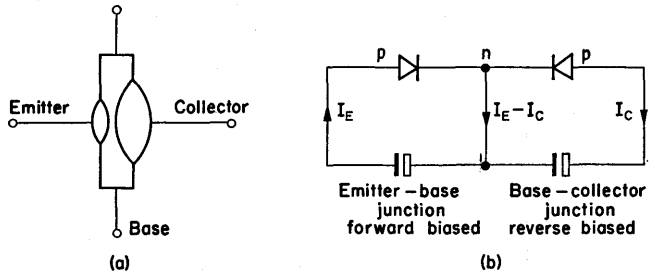



Fig. 2.3. (a) Schematic representation of an alloy transistor. (b) Representation of a *pnp* transistor by two diodes. $I_E$ is the emitter current, $I_C$ is the collector current and the base current $I_B = I_E - I_C$.

and very thin. As the names suggest, the emitter roughly corresponds to the cathode of a thermionic valve, and the collector to the anode. A *pnp* transistor is one in which the emitter and collector are *p* type materials and the base is *n* type. There is a *pn* junction between emitter and base, and an *np* junction between base and collector, so it may be represented by two diodes as in Fig. 2.3b. With the batteries connected as shown, the emitter–base junction is forward biased, thus reducing the potential

barrier, while the base–collector junction is reverse biased and its potential barrier therefore increased, as illustrated in Fig. 2.4. The forward bias of the emitter–base junction causes holes to be injected into the base where, since the base is *n* type, they are minority carriers. Provided that they do not recombine with

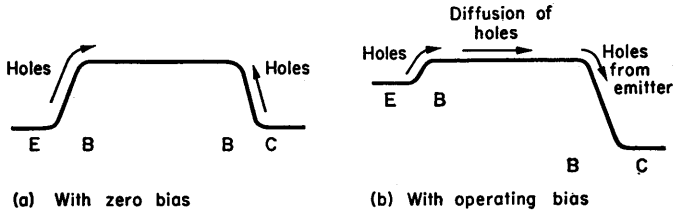



FIG. 2.4. Potential diagrams of a *pnp* transistor showing the effect of biasing. The potential barriers are drawn as hills which the holes have to surmount.

electrons in the base region, these holes will diffuse towards the base–collector junction. This junction is, however, forward biased for such minority carriers, which are swept into the collector region and give rise to a current in the collector circuit.

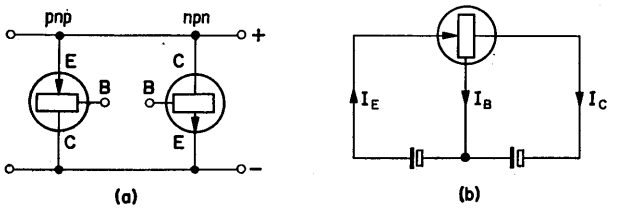



FIG. 2.5. (a) Diagrammatic representation of *pnp* and *npn* transistors. (b) Representation of the fundamental current relationships in a junction transistor.

Not all the holes flowing from the emitter into the base will pass into the collector region as a small proportion will recombine with electrons in the *n* type base. This loss of charge in the base layer is made good by a flow of base current. Varying

the base current varies the voltage across the emitter junction, and so controls the emitter–collector current.

The action of an *npn* transistor is similar, except that the minority carriers through the base region are electrons instead of holes. Whichever type of transistor is used, it is necessary that the emitter–base junction be forward biased, that is, with the supply negative connected to device *n* and the supply positive connected to device *p*. Likewise, the base–collector junction must have reverse bias. This means that a *pnp* transistor has its collector taken to negative while an *npn* type has its collector taken to positive. Since in thermionic valve circuits it is conventional to draw the positive rail at the top of the circuit diagram, in this book this convention is maintained for transistor circuits also. The two types of transistors are therefore represented diagrammatically as in Fig. 2.5a.

## 2.4. Fundamental Current Relationships

In Fig. 2.5b,

$$I_E = I_B + I_C. \tag{2.1}$$

Let

$$\Delta I_B = i_b,$$

$$\Delta I_C = i_c,$$

$$\Delta I_E = i_e.$$

Let the symbol $\alpha$ denote the ratio between collector current and emitter current thus, $\alpha = i_c/i_e$. This will be less than unity, since $i_c$ is less than $i_e$ because of recombination of the minority carriers in the base region. A typical value for $\alpha$ (*the short circuit current gain*) is 0·98.

When a circuit is arranged such that the signal enters at the emitter and is recovered at the collector, the transistor is said to be in *common base* operation. Since $i_b = i_e - i_c$,

$$\frac{i_c}{i_b} = \frac{i_c}{i_e - i_c} = \frac{\alpha}{1 - \alpha}.$$

The ratio between collector current and base current is denoted by the symbol $\beta$:

$$\beta = \alpha/(1 - \alpha) \quad (\beta = 49 \text{ for } \alpha = 0{\cdot}98).$$

Usually $\beta$ ranges from 10 to 150. This implies a current gain if the signal current enters at the base and is recovered at the collector. A transistor used in this way is said to be in *common emitter* operation. This is the most frequently used mode of operation, because of the current gain which may be achieved in this way.

In common emitter operation, the leakage current $I_{CEO}$ that flows (when $I_E = 0$) is approximately $\beta I_{CBO}$. That is, $\beta$ times the leakage current in common base operation. As the collector current is small, and current gain is a function of collector current (low for small currents), the effective $\beta$ will be of the order of half the usual value. Thus, in the case where $\alpha = 0{\cdot}98$ and $\beta = 49$, if $I_{CBO} = 5\ \mu A$, then $I_{CEO} \doteqdot 125\ \mu A$.

## 2.5. Elementary Considerations of Frequency Effects[7]

Charge carriers take a finite time to diffuse through the base and this causes a reduction in current gain at high frequencies. If the current gain at zero frequency $\alpha_0 = i_c/i_e$, then

$$\alpha = \alpha_0 \Big/ \left(1 + \frac{jf}{f_\alpha}\right), \tag{2.2}$$

with reasonable accuracy, where $f_a$ is the frequency at which the gain falls to $0{\cdot}7\alpha_0$. Similarly, since $\beta = \alpha/(1 - \alpha)$,

$$\beta = \beta_0 \Big/ \left(1 + \frac{jf}{f_\beta}\right), \tag{2.3}$$

where $\beta$ falls to $0{\cdot}7\beta_0$ at $f_\beta = (1 - \alpha) f_a$. This is illustrated for the OC206 in Fig. 2.6.

The curve for the short circuit current gain follows closely the

locus of a passive lag (a capacitor shunted by a resistor) up to a frequency of $f_\alpha/2$. This relationship is used by Ebers and Moll in switching analysis.[8] The common emitter short circuit current gain $\beta$ can be obtained from Fig. 2.6b. It falls from $\beta_0$ to

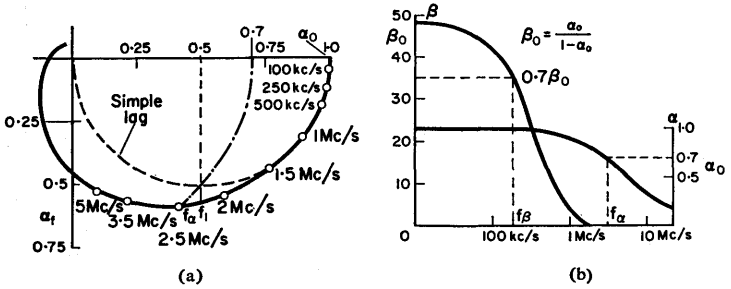



FIG. 2.6. Variation of short circuit current gain $\alpha$ with frequency, for an OC206. Up to 1.5 Mc/s the curve for $\alpha$ closely follows that of a passive lag.

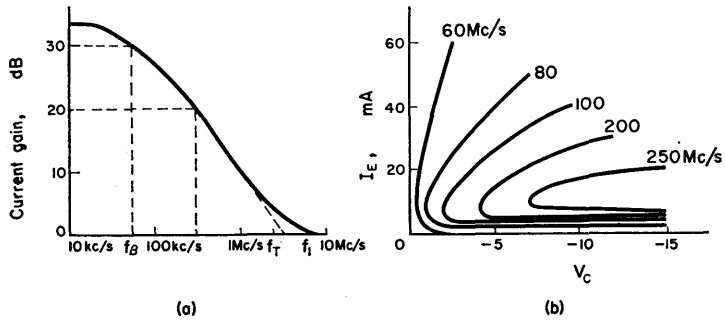



FIG. 2.7. (a) Curve showing relationship between $f_\beta$, $f_T$ and $f_1$. For $f_T = 3$ Mc/s and $\beta = 10$ (20 dB), bandwidth $= f_T/\beta = 300$ kc/s. (b) Variation in gain-bandwidth product, with operating conditions, for a high frequency transistor.

$0{\cdot}7\beta_0$ at approximately $(1 - \alpha)f_\alpha$, and to unity at $\alpha_R = 0{\cdot}5$. This latter frequency is known as $f_1$:

$$f_1 = \frac{f_\alpha}{1 + \varphi}, \tag{2.4}$$

where $\varphi = 0{\cdot}2$ for homogeneous base transistors and varies between 0·2 and unity for graded base transistors (§ 2.8).

*Gain-bandwidth Product $f_T$*[7]

If $\beta$ is plotted against frequency, both on logarithmic scales, the relationship is as shown in Fig. 2.7a. The gain-bandwidth product $f_T$ is obtained by projecting the straight section of the curve to intercept the unity gain line (0 dB). It can thus be determined by finding $\beta$ at any frequency on the 20 dB/decade slope and multiplying this value by the frequency at which it is measured. Thus, in Fig. 2.7a, $f_T = 3$ Mc/s, and, at 20 dB ($\beta = 10$) the bandwidth is 300 kc/s. The gain-bandwidth product varies with operating conditions, as illustrated in Fig. 2.7b.

## 2.6. Voltage Breakdown[9]

When the reverse voltage applied to a junction is increased above a certain figure a "breakdown" will occur and the reverse resistance will fall from the usual high value to a low one. This, in itself, will not damage the unit, but it is possible, under the breakdown condition, for large currents to flow if there is no controlling external resistance.

The three mechanisms of breakdown are:

(a) Punch through.
(b) Zener.
(c) Avalanche.

*(a) Punch Through*

The width of the depletion layer of a reverse biased junction is approximately proportional to the square root of the voltage, and it is possible for it to extend to the emitter junction. This provides a way for holes to reach the collector, independent of the base, and causes a short circuit between emitter and collector. Thin based transistors, such as surface barrier types, have voltage

limitations due to punch through, typically having punch through values of $V_{PT} = -5$ V.

*(b) Zener Breakdown*

This occurs when the number of added impurities is high (the *n* and *p* materials have low resistivity). Application of reverse bias can cause the valence band of the *p* material to overlap the conduction band of the *n* material and the junction will break down. This is usually of no significance in the case of transistors where the doping levels are low, but the phenomenon is usefully employed in Zener and tunnel diodes. Zener breakdown is usually confined to below 10 V.

*(c) Avalanche*

In lightly doped junctions, carriers entering the depletion layer are accelerated by the field set up by the collector–base voltage. If this voltage is high enough, the carriers can ionize fixed atoms giving rise to hole–electron pairs which, in turn, can cause further ionization. The voltage at which this happens is the "avalanche voltage".

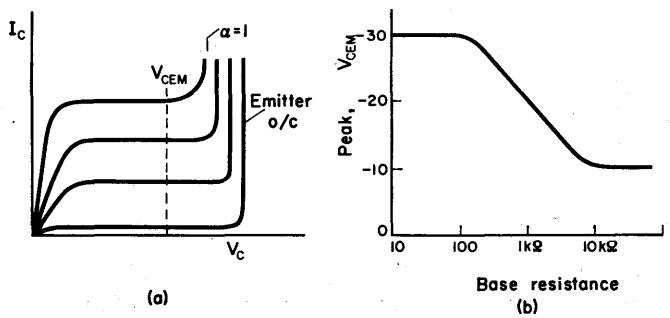



FIG. 2.8. (a) Typical collector characteristic, with $V_C$ extended into the breakdown region, for common base operation. (b) Maximum permissible collector voltage, for a given base resistance, with transistor in common emitter connection.

The maximum collector voltage rating is frequently low for applications where the base resistance is high, and is a minimum for open circuited base $V_{CEM}$. The maximum collector rating is $V_{CBM}$ which is the collector–base voltage with emitter open circuit. In pulse circuits, the base–emitter junction is frequently reverse biased, and there is similarly a maximum reverse voltage $V_{BEM}$.

Typical values for a transistor could be:

$$V_{CEM} = 40\text{ V}; \quad V_{CBM} = 20\text{ V}; \quad V_{BEM} = 6\text{ V}.$$

In most applications a safe working voltage will be between $V_{CEM}$ and $V_{CBM}$.

In Fig. 2.8a is plotted a typical collector characteristic with $V_C$ extended into the breakdown region. Figure 2.8b illustrates how the maximum peak collector voltage, for an OC122, varies with base resistance.

## 2.7. Power Dissipation[10]

In a transistor most power dissipation occurs in the collector–base junction where the voltage gradient is a maximum. Using peak instantaneous values, collector dissipation,

$$P_C \doteqdot v_{CE} i_C \doteqdot \frac{T_{JM} - T}{\theta}, \tag{2.5}$$

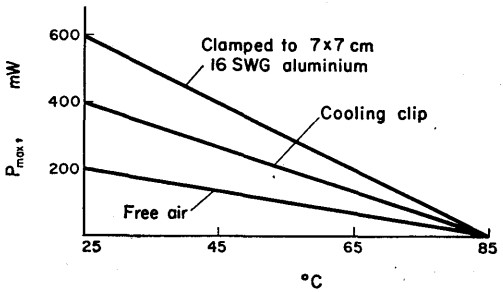



Fig. 2.9. The use of a heat sink reduces the thermal resistance $\theta$, and thus increases the maximum permissible dissipation for a given transistor.

where $T_{JM}$ is the maximum junction temperature, $T$ is the ambient temperature, and $\theta$ is the rise in temperature, for a given unit of power dissipation (thermal resistance).

EXAMPLE. Ambient temperature 35°C, $T_{JM} = 70°C$ and $\theta = 1°C/mW$,

$$P_C = \frac{35°C}{1°C/mW} = 35 \text{ mW}.$$

Figure 2.9 illustrates how the use of a heat sink reduces the value of $\theta$ for a given transistor.

## 2.8. SUMMARY OF TRANSISTOR TYPES

### *Low and Medium Frequency Types*

Two general processes are employed, (a) alloy, and (b) grown junction. Alloy types have a low collector resistance when bottomed and are suitable for amplifiers and switches at low and high powers. However, $f_1$ is limited to approximately 20 Mc/s and beyond this frequency base thinness leads to mechanical weakness.

### *Medium to High Frequency Types*

Most new techniques are developing devices in this category, providing values of $f_1$ between 20 and 1000 Mc/s.

### *Surface Barrier*

Historically, the first mass produced h.f. transistor, the surface barrier type, uses an accurately controlled etching process to produce a very thin base upon which the emitter and collector are electro-deposited. The main limitation is low punch through voltage (6 V), and this manufacturing technique has been superseded by the micro-alloy process.

*Diffused Base*

These are sometimes known as Graded Base, or Drift Transistors. By varying the resistivity of the base material, an electric field is formed which causes the charge carriers to drift across the base, rather than diffuse across, as with a homogeneous base. This reduces the transit time and consequently increases the upper frequency limit.

*Mesa*

The device is built up on material that forms the collector, and opposite type material is diffused in to form the base. Two strips are alloyed on to the diffused region, one forming the emitter and the other the base contact. The narrow base width provides a high $f_1$, and the collector allows high power dissipation.

*Epitaxial Mesa*

The disadvantage of the Mesa transistor is the large carrier storage which limits switching speed, and the high saturation resistance. Both these limitations are overcome in the epitaxial mesa, by laying a high resistance region on a low resistance substrate, as illustrated in Fig. 2.10.

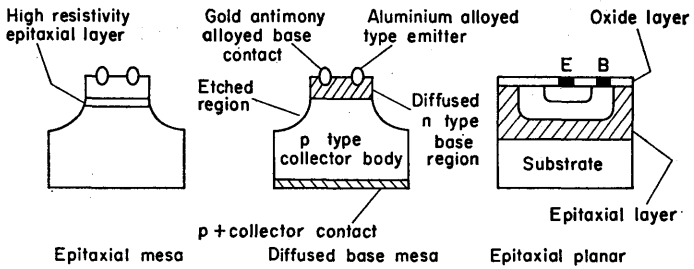



FIG. 2.10. Construction of three widely used transistor types. Compared with the alloy device of Fig. 2.3, the larger collector volume permits much greater dissipation.

*Planar*

Using silicon as the substrate, the surface is passivated by oxidization, and diffusion is carried out through etched areas. Such a technique reduces leakage current and provides high gain at low current levels. Because of surface passivation the shoulders do not have to be etched away, as is done in the mesa transistor.

## 2.9. Static Characteristics of the Junction Transistor

In normal operation the input junction of a transistor is forward biased and, unlike the idealized valve, power has to be supplied to the input terminals. The output current is consequently a function of both the input current and voltage.

*Input Characteristics*

In Fig. 2.11 curves are plotted of base current against base voltage, with collector voltage constant, for the common emitter mode of operation.

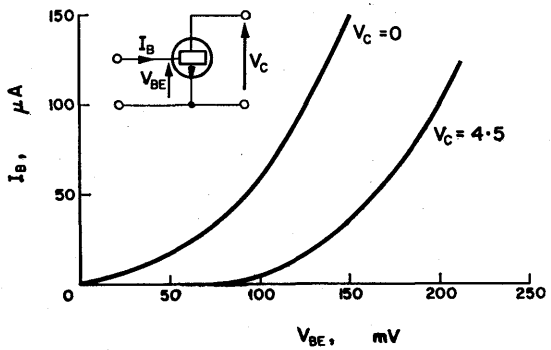



FIG. 2.11. The input characteristic.

Differential input resistance $h_i = \left[\frac{\delta V_B}{\delta I_B}\right]$ ($V_C$ constant).

Let the differential input resistance be denoted by the symbol $h_i$, such that

$$h_i \underset{\text{def}}{=} \left[\frac{\delta V_B}{\delta I_B}\right] \quad (V_C \text{ constant}). \tag{2.6}$$

Then on the input characteristic curve the slope at any working point is equal to the reciprocal of $h_i$. It is apparent that the input curves are a function of the collector voltage. The input resistance does not change greatly with collector voltage but varies widely with base voltage. Typical operating values of $h_i$ are in the range 500–2000 Ω for small units.

*The Transfer Characteristic*

This relates output current to input current and is linear except for very small and very large currents (Fig. 2.12).

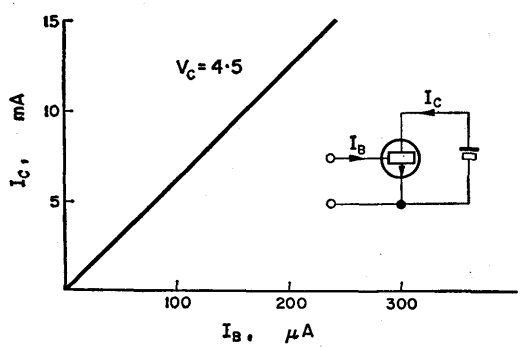



FIG. 2.12. The transfer characteristic. This is linear except for very small and very large currents. The slope of this graph is the current gain, $h_f = \left[\frac{\delta I_B}{\delta I_C}\right]$ ($V_C$ constant).

The slope of the transfer characteristic is the current gain, which for the common emitter case is defined as

$$h_f \underset{\text{def}}{=} \left[\frac{\delta I_C}{\delta I_B}\right] \quad (V_C \text{ constant}) \text{ previously denoted by } \beta. \tag{2.7}$$

Both the input and transfer characteristics can be easily measured in the laboratory by supplying the input current from a constant current generator.

*The Output Characteristic*

A family of curves is drawn (Fig. 2.13) relating collector current to collector voltage with base current as parameter. This can be used in the same manner as the thermionic valve anode characteristics in which grid voltage is the parameter.

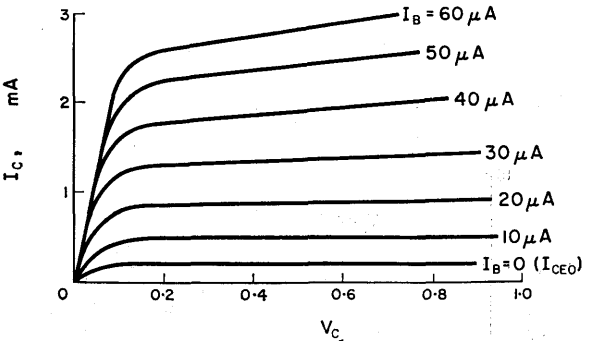



FIG. 2.13. The output characteristic.

Output conductance $h_o = \left[\frac{\delta I_C}{\delta V_C}\right]$ ($I_B$ constant).

The slope of the curves is the output conductance, defined as:

$$h_o \underset{\text{def}}{=} \left[\frac{\delta I_C}{\delta V_C}\right] \quad (I_B \text{ constant}). \tag{2.8}$$

It is commonly of the order of $50 \times 10^{-6}$ mho.

*Voltage Feedback Characteristic*

The fourth relationship is between output and input voltage and is the voltage feedback characteristic. The slope of this

curve is:

$$h_r \underset{\text{def}}{=} \left[\frac{\delta V_B}{\delta V_C}\right] \quad (I_B \text{ constant}). \tag{2.9}$$

Voltage feedback ratios are typically of the order of $5 \times 10^{-4}$.

## 2.10. Small Signal Representation

### *Hybrid Equivalent Circuit*

This representation makes use of $h$ parameters. For given operating conditions and small signals, the network of Fig. 2.14 represents a transistor at low frequency.

The equations of this network are:

$$v_1 = h_{11}i_1 + h_{12}v_2, \tag{2.10}$$

$$i_2 = h_{21}i_1 + h_{22}v_2. \tag{2.11}$$

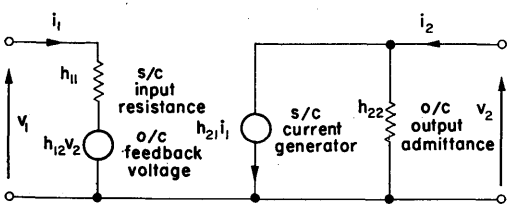



FIG. 2.14. Small signal representation of a transistor by a hybrid equivalent network. A voltage generator is used in the input circuit, and in the output circuit a current generator is employed.

And, in matrix form,

$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}, \tag{2.12}$$

where

$$\text{(a) } h_{11} = h_i = \left[\frac{\delta V_{\text{in}}}{\delta I_{\text{in}}}\right] \quad (V_C \text{ constant}), \tag{2.13}$$

$$= \frac{v_1}{i_1} \text{ when } v_2 \text{ is zero},$$

that is when the output is short circuited for signal currents;

$$\text{(b) } h_{12} = h_r = \left[\frac{\delta V_{\text{in}}}{\delta V_{\text{out}}}\right] \quad (I_B \text{ constant}), \tag{2.14}$$

$$= \frac{v_1}{v_{\text{out}}} \text{ when } i_1 \text{ is zero,}$$

that is when the input is open circuited;

$$\text{(c) } h_{21} = h_f = \left[\frac{\delta I_{\text{out}}}{\delta I_{\text{in}}}\right] \quad (V_C \text{ constant}), \tag{2.15}$$

$$= \frac{i_2}{i_1} \text{ when } v_2 \text{ is zero,}$$

that is when the output is short circuited;

$$\text{(d) } h_{22} = h_{\text{out}} = \left[\frac{\delta I_{\text{out}}}{\delta V_{\text{out}}}\right] \quad (I_B \text{ constant}), \tag{2.16}$$

$$= \frac{i_2}{v_2} \text{ when } i_1 \text{ is zero,}$$

that is when the input is open circuited.

The values of these $h$ parameters will vary according to the mode of operation of the transistor. To denote which mode is in use a second subscript, $e$, $b$ or $c$, is added to the $h$ symbol. Thus,

$h_{ie}$ = Input impedance, common emitter.
$h_{rb}$ = Voltage feedback ratio, common base.
$h_{oc}$ = Output admittance, common collector.
$h_{fe}$ = Forward current transfer ratio, common emitter.

*T Representation*

In this representation of the transistor the component parts retain their identity in all configurations and this enables a rapid appreciation of a network to be made (see Fig. 2.15a).

It is possible to obtain the values of $r$ parameters from known $h$ parameters, and vice versa.

EXAMPLE. (See Fig. 2.15b.)

$h_{11} = h_{ie}$ for common emitter operation,
$= v_1/i_1$ with output short circuited.

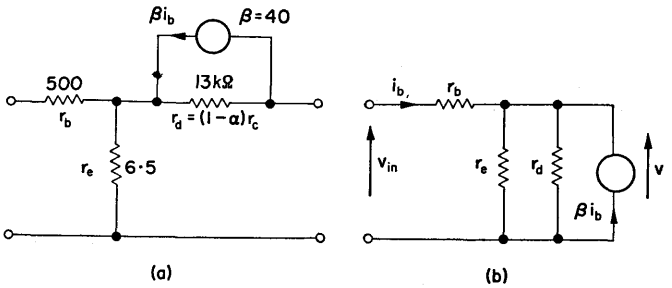



FIG. 2.15. (a) $T$ representation for common emitter operation, using $r$ parameters. (b) The output is short circuited for the determination of $h_{11}$ from $r$ parameters.

Then,

$$i_b = v\left[\frac{1}{r_e} = \frac{1}{r_d}\right] - \beta i_b,$$

and

$$v = i_b(1 + \beta)\left[\frac{r_e \cdot r_d}{r_e + r_d}\right],$$

also,

$$v_i = v + i_b r_b.$$

Therefore

$$h_{11} = r_b + (1 + \beta)\left[\frac{r_e \cdot r_d}{r_e + r_d}\right].$$

Therefore

$$h_{11} \doteqdot r_b + r_e \quad \text{since } r_d \text{ is much greater than } r_e.$$

In Table 2.1 is given the relationships between $h$ and $r$ parameters, in both exact and approximate form. Using these approximations, $r$ parameters may readily be obtained in terms

of $h$ parameters. For example, in terms of common emitter parameters,

$$r_e = \frac{h_{re}}{h_{oe}}, \quad r_c = \frac{1 + h_{fe}}{h_{oe}}, \quad \alpha = \frac{h_{fe}}{1 + h_{fe}}, \quad \beta = h_{fe},$$

$$r_b = h_{ie} \frac{h_{re}}{h_{oe}} (1 + h_{fe}) = h_{ie} - h_{re} r_c.$$

## 2.11. Transistor Biasing[11]

For operation the emitter–base junction must be forward biased. This is different to the thermionic valve which can operate with the grid–cathode reversed biased and consequently drawing zero current.

The simplest bias method is to supply a base current which will allow the required operating conditions. (See Fig. 2.16.)

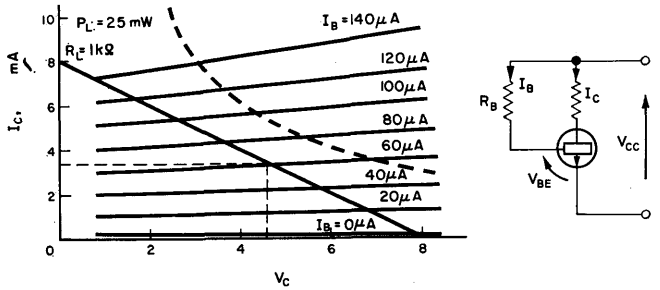



FIG. 2.16. Determination of the necessary bias current for a given operating condition. Note that the operating point must lie below the curve indicating maximum permissible collector dissipation.

*Base Current Biasing*

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}. \tag{2.17}$$

Since $V_{BE}$ is very much less than $V_{CC}$, $I_B \doteqdot V_{CC}/R_B$.

TABLE 2.1

| Exact | Approximate, $r_d \gg r_b, r_e$ |
|---|---|
| $h_{ie} = \dfrac{\Delta}{r_e + r_d}$ | $r_b + \dfrac{r_e}{1-\alpha}$ |
| $h_{ib} = \dfrac{\Delta}{r_b + r_c}$ | $r_e + r_b(1-\alpha)$ |
| $h_{ic} = \dfrac{\Delta}{r_e + r_d}$ | $r_b + \dfrac{r_e}{1-\alpha}$ |
| $h_{fe} = \dfrac{-(r_e - \alpha r_c)}{r_e + r_d}$ | $\dfrac{\alpha}{1-\alpha}$ |
| $h_{fb} = \dfrac{-(r_b + \alpha r_c)}{r_c + r_b}$ | $-\alpha$ |
| $h_{fc} = \dfrac{-r_c}{r_c + r_d}$ | $-\dfrac{1}{1-\alpha}$ |
| $h_{re} = \dfrac{r_e}{r_e + r_d}$ | $\dfrac{r_e}{r_d}$ |
| $h_{rb} = \dfrac{r_b}{r_b + r_c}$ | $\dfrac{r_b}{r_c}$ |
| $h_{rc} = \dfrac{r_d}{r_e + r_d}$ | $1$ |
| $h_{oe} = \dfrac{1}{r_e + r_d}$ | $\dfrac{1}{r_d}$ |
| $h_{ob} = \dfrac{1}{r_b + r_c}$ | $\dfrac{1}{r_c}$ |
| $h_{oc} = \dfrac{1}{r_e + r_d}$ | $\dfrac{1}{r_d}$ |

Where $\Delta = r_e r_b + r_c[r_e + r_b(1-\alpha)]$
$= r_e(r_b + r_c) + r_b r_d,$
and $r_d = r_c(1-\alpha)$

Thus, for $R_L = 1\,\text{k}\Omega$ and $V_{CC} = 8\,\text{V}$, for a bias current of 60 $\mu$A,

$$R_B = \frac{V_{CC}}{I_B} = \frac{8\,\text{V}}{60\,\mu\text{A}} = 133\,\text{k}\Omega.$$

$I_C = BI_B + I_{CEO}$, where $B$ is the large signal current gain.

$$B = \frac{I_C - I_{CEO}}{I_B} = 57 \text{ in this case.} \qquad (2.18)$$

The small signal current gain $\beta$, evaluated at the working point, is 52, showing that the error involved in using $\beta$ in place of $B$ is negligible.

*Advantages of current biasing*

1. Simplicity and small number of components required.
2. Biasing is largely independent of $V_{BE}$, the base–emitter voltage. The $V_{BE}$ required to maintain a given collector current falls with increasing temperature. If $V_{BE}$ is very much less than $V_{CC}$ (or $V_{BB}$) the bias current $I_B$ is largely indepedent of $V_{BE}$.

*Disadvantages*

1. $I_{CEO}$ is not controlled and can limit the collector swing or even bottom the transistor in extreme conditions. ($I_{CEO}$ is doubled for each 8 °C rise in temperature.)

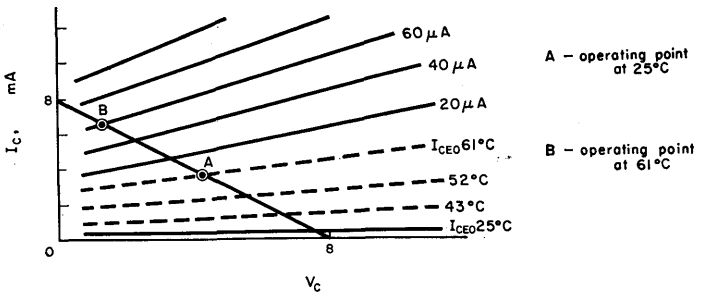



FIG. 2.17. Change in operating point due to increasing temperature, for a germanium transistor with base current biasing.

2. The current gain increases with temperature and can vary greatly with different transistors. Since the standing current $I_C = \beta I_B + I_{CEO}$, the working point can also differ. This is illustrated in Fig. 2.17.

In spite of the disadvantages, current biasing is very useful, especially for experimental work. The change in operating point is greatly reduced if large collector currents are used (so that $I_{CEO}$ is only a small fraction of $I_C$), and the loads are small.

*Collector Feedback Biasing*

Ideally, the transistor should be biased by a method which prevents excessive shift of the working point, due to temperature changes. Indeed, in the absence of such stabilization, or where the stabilization is insufficient, thermal runaway may result. Thermal runaway occurs when an increase in temperature causes an increase in collector current, which in turn results in a further increase in temperature. The effect is cumulative and can result in the destruction of the transistor, although it normally only occurs in high power stages.

The circuit of Fig. 2.18a is the simplest method of providing a degree of stabilization to the operating point.

The performance equations of this circuit are:

$V_C \doteqdot V_{CC} - I_C R_C$ (neglecting $I_B$ in comparison with $I_C$),

$I_C = \beta I_B + I_{CEO}$,

$I_B \doteqdot V_C / R_{BC}$ (neglecting $V_{BE}$ in comparison with $V_C$).

Combining these equations,

$$I_C \doteqdot \frac{\beta V_{CC}}{R_{BC} + \beta R_C} + \frac{I_{CEO} \cdot R_{BC}}{R_{BC} + \beta R_C}. \tag{2.19}$$

Differentiating with respect to the leakage current $I_{CEO}$,

$$\frac{\delta I_C}{\delta I_{CEO}} = \frac{1}{1 + \beta R_C / R_{BC}}. \tag{2.20}$$

That is, a change $\delta I_{CEO}$ causes a change of $(1/K)\,\delta I_C$, where

$$\frac{1}{K} = \frac{1}{1 + \beta R_C/R_{BC}}. \tag{2.21}$$

The factor $K$ is the stabilization factor and should obviously be as large as possible. In this case this is achieved by using a transistor with a large $\beta$.

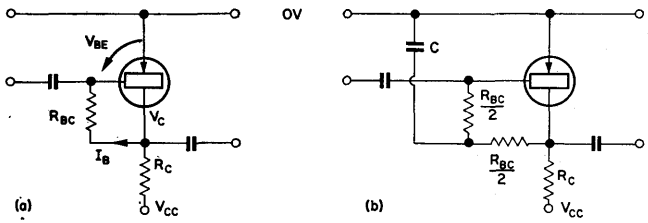



FIG. 2.18. (a) Stabilization of the operating point using collector feedback biasing. (b) The feedback resistor is decoupled to eliminate loss in gain due to negative feedback.

*Calculation of $R_{BC}$*

If, as in the previous example,

$$\beta = 57,\ R_C = 1\ \text{k}\Omega,\ I_B = 60\ \mu\text{A} \quad \text{and} \quad V_C = 4{\cdot}5\ \text{V},$$

$$R_{BC} = V_C/I_B = 4{\cdot}5\ \text{V}/60\ \mu\text{A} = 75\ \text{k}\Omega.$$

This provides a stabilization factor $K = 1 + \beta R_C/R_{BC} = 1{\cdot}75$.

*Disadvantages*

1. The collector current must always be greater than $I_{CEO}$.
2. There is negative feedback at signal frequency unless decoupling is employed, as in Fig. 2.18b.
3. The degree of stabilization is relatively small.

The method is applicable for amplifiers in which overall signal inversion occurs. It has the advantage that only one

capacitor is used and consequently introduces only one additional time constant. This is a very important consideration in the case of feedback amplifiers. This form of biasing can be applied over more than one stage, for amplifiers that have overall signal inversion, as shown in Fig. 2.19.

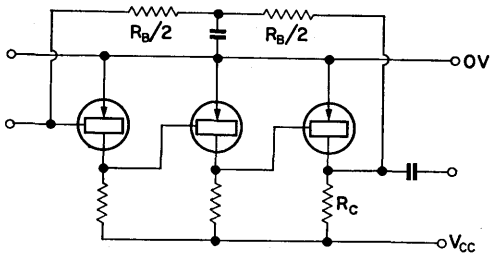



FIG. 2.19. A three-stage amplifier with feedback stabilization. If the collector voltage of the output transistor is half $V_{CC}$, the stabilization factor is $K = 2$.

*Emitter Resistor Stabilization*

This method is generally used with a voltage dividing network to provide the base voltage, and is similar to cathode bias used to stabilize the operation of a thermionic valve. Referring to the

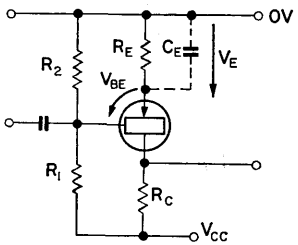



FIG. 2.20. Emitter resistor stabilization. The capacitor $C_E$ decouples $R_E$ to prevent loss in gain due to negative feedback.

circuit of Fig. 2.20, the base voltage is set by the voltage divider consisting of $R_1$ and $R_2$:

$$I_E = V_E/R_E = (V_B - V_{BE})/R_E \doteqdot V_B/R_E,$$

where $V_B$ is much greater than $V_{BE}$. ($V_B$ is usually of the order of 10 $V_{BE}$.)

If $R_1$ and $R_2$ are very small and $R_E$ is very large, the circuit is indistinguishable from the common base configuration. The leakage current is then $I_{CBO}$ (not $I_{CEO}$) and of the order of 10 μA, and $I_C = I_E + I_{CO}$.

Over a wide temperature range $\alpha$ only changes by a small percentage and hence a good degree of stabilization is obtained.

The circuit may be represented by Fig. 2.21, in which

$$R_B = R_1R_2/(R_1 + R_2).$$

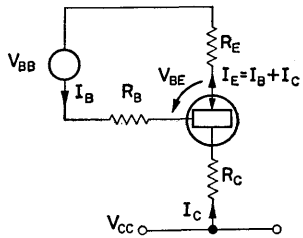



FIG. 2.21. Equivalent representation for determining the stabilization factor.

Then, providing $R_C$ and $R_E$ are not very large,

$$I_C \doteqdot I_{CEO} + \beta I_B, \tag{2.22}$$

$$I_E = I_C + I_B, \tag{2.1}$$

$$I_B = \frac{V_{BB} - (V_{BE} + R_E I_E)}{R_B}. \tag{2.23}$$

From these three equations,

$$I_B = \frac{V_{BB}}{R_E + R_B} - \frac{V_{BE} + R_E I_C}{R_E + R_B}, \tag{2.24}$$

and

$$I_C = \frac{I_{CEO}}{K} + \frac{\beta V_{BB}}{R_E + R_B} \cdot \frac{1}{K} \tag{2.25}$$

if $V_{BE}$ is much less than $V_E$, and where

$$K = 1 + \frac{\beta R_E}{R_E + R_B}. \tag{2.26}$$

Differentiating $I_C$ with respect to $I_{CEO}$,

$$\frac{\delta I_C}{\delta I_{CEO}} = \frac{1}{K}. \tag{2.27}$$

$K$ is thus the stabilization factor, and if $R_E$ is very much greater than $R_B$, approximates to $1 + \beta$. The designer can thus select his degree of stabilization by suitable choice of values for $R_E$ and $R_B$.

DESIGN EXAMPLE 2.1

Required, a peak output signal of 3 V without distortion. From the collector characteristic, let the operating point chosen to suit this requirement be $V_C = -8$ V and $I_C = 3$ mA, for a transistor operating from a supply of $-12$ V. The collector voltage swing is from $-5$ to $-11$ V, so a maximum of 5 V is available for $V_E$, which should be somewhat less than this figure. Let $V_E$ be $-3$ V so that, for $I_C = 3$ mA, $R_E = 1$ kΩ.

The ratio $R_B/R_E$ is chosen according to the degree of stabilization required. If $R_B/R_E = 3$,

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = 3 \text{ k}\Omega. \tag{2.28}$$

As $I_B$ is usually small, $V_B \doteqdot V_{CC} \cdot R_2/(R_1 + R_2)$. But $V_B = V_{BE} + V_E$ and since $V_{BE}$ is much less than $V_E$,

$$V_B \doteqdot \frac{R_2}{R_1 + R_2} \cdot V_{CC} \doteqdot V_E. \tag{2.29}$$

Therefore

$$\frac{12R_2}{R_1 + R_2} = 3 \quad \text{and} \quad R_1 = 3R_2.$$

Substituting in eqn. (2.28), $R_2 = 4\,\text{k}\Omega$ and $R_1 = 12\,\text{k}\Omega$. Make them 4·7 kΩ and 12 kΩ, which are preferred values. To give the required $V_C$, $R_C = 4\text{ V}/3\text{ mA} \doteqdot 1{\cdot}2\,\text{k}\Omega$, and the circuit is as shown in Fig. 2.22. A smaller value of $R_B$ would increase the stability, but would:

(1) draw extra current from the power supply,
(2) reduce the amplifier input resistance and provide a lower resistance shunt path for input signal current.

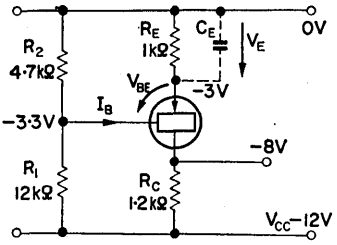



FIG. 2.22. Circuit of Design Example 2.1.

For most a.c. applications $R_E$ is decoupled with a capacitor to eliminate negative feedback. $R_E$ in effect increases $r_e$ to $R_E + r_e$ and the input resistance from (approximately) $r_b + \beta r_e$ to $r_b + \beta(r_e + R_E)$, which reduces the voltage gain.

## 2.12. TRANSISTOR AMPLIFIER CHARACTERISTICS[12]

The three different modes of operation, illustrated in Fig. 2.23, have widely different characteristics, and these are now compared so that a designer may select the mode most suitable for a given application.

### *Current Gain*

Common base short circuit current gain $= \alpha = -h_{21} = -h_{fb}$ $= 0{\cdot}98$. Common emitter short circuit current gain $= \beta = h_{21}$ $= h_{fe} = 49$. Common collector short circuit current gain $= 1 + \beta = h_{21} = h_{fc} = 50$.

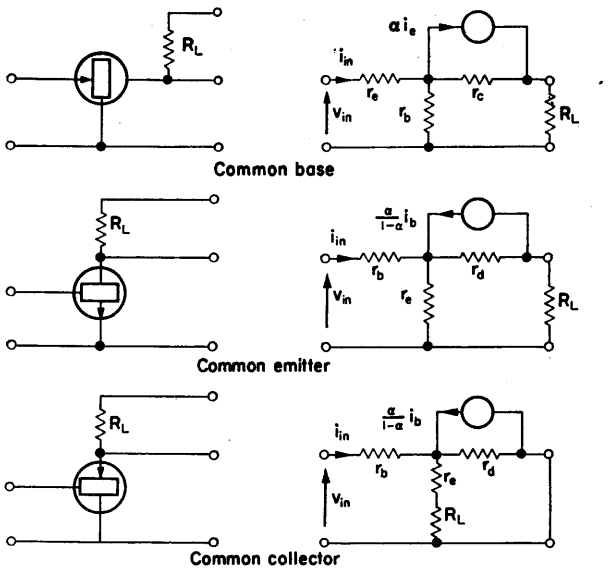



FIG. 2.23. Forms of transistor operation. The common emitter arrangement is the one most frequently used since it can provide current, voltage and power amplification.

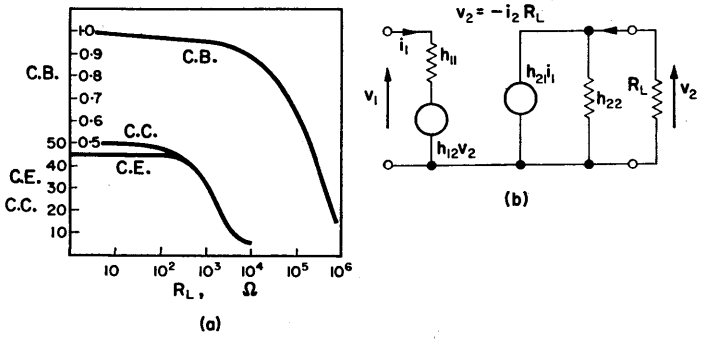



FIG. 2.24. (a) Current gain as a function of load for the three modes of operation. Note that for the common collector arrangement the current gain is much greater than for common base. (b) Hybrid equivalent network which is the same for all modes of operation.

The way in which current gain varies, as the load resistor $R_L$ is increased, is shown in Fig. 2.24a. Referring to the hybrid network of Fig. 2.24b,

$$\frac{i_2}{i_1} = \frac{h_{21}G_L}{h_{22} + G_L}. \tag{2.30}$$

From the short circuit value, current gain falls by half when $G_L = h_{22}$.

Typical values for $h_{22}$ are 1 MΩ for common base operation and 20 kΩ for common emitter.

*Voltage Gain*

$$v_2 = \frac{-h_{21}}{h_{22} + G_L} i_1 = \frac{-h_{21}}{h_{22} + G_L} \cdot \frac{v_1 - h_{12}v_2}{h_{11}}. \tag{2.31}$$

Thus,

$$\frac{v_2}{v_1} = \frac{-h_{21}}{h_{22}h_{11} - h_{12}h_{21} + h_{11}G_L} = \frac{-h_{21}}{\Delta h + G_L h_{11}}, \tag{2.32}$$

where

$$\Delta h = h_{22}h_{11} - h_{12}h_{21}.$$

To obtain an approximate value for voltage gain the term $h_{12}v_2$ can frequently be omitted since the voltage feedback ratio $h_{12}$

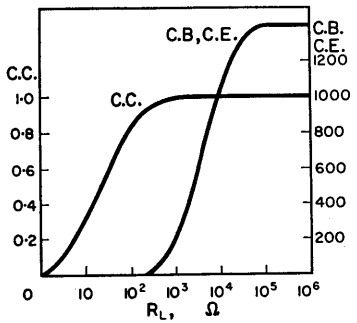



FIG. 2.25. Voltage gain as a function of load resistance. The common collector gain is less than unity, while that of the common base and common emitter arrangements is very much greater.

is small. Variation of voltage gain with load resistance is plotted in Fig. 2.25.

*C.B. Input Resistance*

Referring to the $T$ equivalent network of Fig. 2.23, and where $R_L$ is small, for the common base connection,

$$v_{in} \doteqdot r_e i_e + r_b(i_e - i_c) = i_e[r_e + (1 - \alpha)\, r_b],$$

where $\alpha$ is the current gain.

$$r_{in} = v_{in}/i_{in} = r_e + (1 - \alpha)\, r_b = h_{ie}. \qquad (2.33)$$

As the current gain falls off for increasing $R_L$, $r_{in}$ tends to $r_e + r_b$.

*C.E. Input Resistance*

$$v_{in} = r_b i_b + r_e(i_e + i_c) = i_b[r_b + r_e(1 + \beta)], \qquad (2.34)$$

if $R_L$ is small, and where $\beta$ is the current gain. Thus $r_{in} = r_b + (1 + \beta)\, r_e$ and tends to $r_b + r_e$ as $R_L$ tends to infinity, as does the input resistance of the common base arrangement.

*C.C. Input Resistance*

$$v_{in} = r_b i_b + (R_L + r_e)\,(i_e + i_c) = i_b r_b + (R_L + r_e)\,(1 + \beta),$$

so that

$$r_{in} = r_b + (R_L + r_e)\,(1 + \beta). \qquad (2.35)$$

Thus, for small values of $R_L$, common collector input resistance is approximately the same as that of the common emitter connection. However, since $R_L$ is in series with $r_e$, for values of $R_L$ between 100 Ω and 10 kΩ, $r_{in}$ is approximately equal to $\beta R_L$. The input resistance of the three modes of operation are compared in Fig. 2.26.

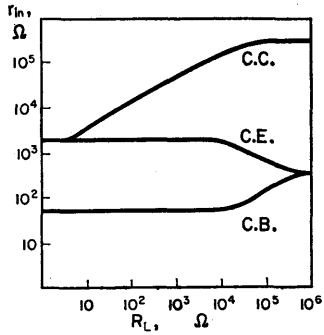



FIG. 2.26. Comparison of input resistance. For common base and common emitter $r_{in}$ tends to the same value $(r_e + r_b)$, as $R_L$ becomes very large. In the common collector mode of operation the input resistance is directly proportional to load resistance over a wide range.

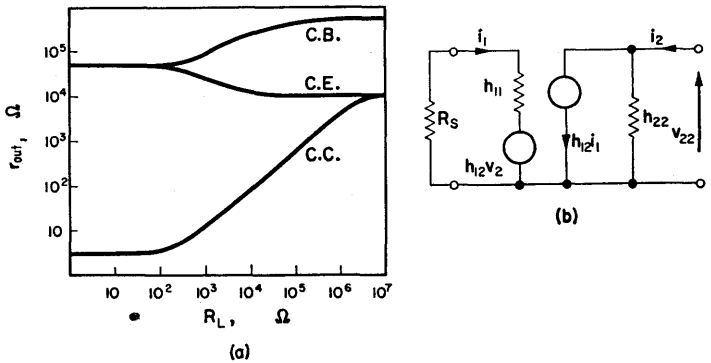



FIG. 2.27. Output resistance as a function of source resistance. $r_{out} = v_2/i_2$, i.e. the resistance seen when looking into the output terminals.

### *Output Resistance*

In common emitter operation the output resistance remains relatively constant as the source resistance $R_S$ changes, but varies considerably for the other two connections.

In Fig. 2.27b, and for common emitter operation, the current generator provides a current which opposes the output current, thus increasing the output resistance when base current flows. The opposite effect occurs with common base and common collector connections:

$$i_1 = \frac{-h_{12}v_2}{h_{11} + R_s} \quad \text{and} \quad i_2 = i_1h_{21} + v_2h_{22}.$$

Thus, output conductance,

$$g_o = \frac{i_2}{v_2} = \frac{-h_{12}b_{21}}{h_{11} + R_s} + h_{22}. \tag{2.36}$$

*Power Gain*

The power gains plotted in Fig. 2.28 are for the case in which the power source is matched to the input resistance of the transistor.

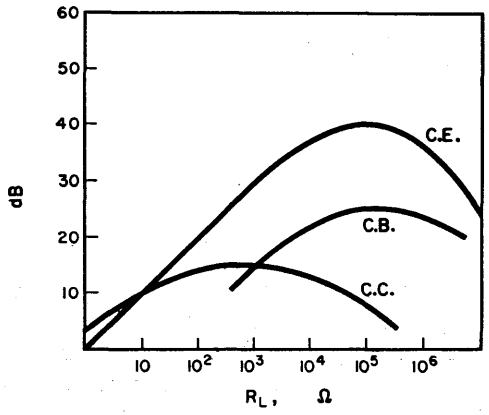



FIG. 2.28. Power gain as a function of load resistance, for the case where the signal source is matched to the input resistance of the transistor.

*Performance of Transistor Amplifiers*

Because of its ability to provide both voltage and current amplification the common emitter configuration is the one generally used in transistor amplifiers. It is also preferred because its input and output resistances are normally of a more

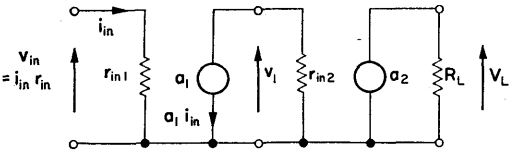



FIG. 2.29. Approximate equivalent network of two transistors in tandem.

useful magnitude and are reasonably constant. In tandem connection the common emitter (due to the current gain) can provide voltage amplification. If $a$ is the current gain of each stage, then, referring to Fig. 2.29,

$$v_1 = -a_1 \cdot r_{in2} \cdot i_{in} = \frac{-a_1 \cdot r_{in2}}{r_{in1}} \cdot v_{in}. \tag{2.37}$$

$$v_L = a_1 a_2 R_L i_{in},$$

$$= \frac{a_1 a_2}{r_{in1}} \cdot R_L v_{in}, \tag{2.38}$$

if $$r_{in1} = r_{in2}.$$

For common emitter operation, if the output and load resistances are equal, the voltage gain is equal to the current gain which will generally approach $\beta$, being in the range 10–80. If the load resistance is very much greater than $r_{in}$ the gain is increased as long as $a_2$ is not significantly reduced.

For common base, with equal input and load resistances, the current gain is less than unity and there will be no voltage gain. If $R_L$ is greater than $r_{in}$ there will be a voltage gain, but stages in tandem provide no increase in gain unless impedance transforma-

tion is provided (transformer connection). For common collector, the input resistance is a function of load resistance, $r_{in} \doteqdot a_1 a_2 R_L$. Thus,

$$v_L \doteqdot \frac{a_1 a_2 R_L}{r_{in1}} \cdot v_{in} \doteqdot \frac{a_1 a_2 R_L}{a_1 a_2 R_L} \cdot v_{in} = v_{in}. \qquad (2.39)$$

## 2.13. EXAMPLES

### (a) *Common Emitter*

Figure 2.30a is a three-stage direct coupled amplifier, each transistor having the $h$ parameters, $h_{21} = \beta = 50$, $h_{11} = 1\ \text{k}\Omega$, $h_{12} = 5 \times 10^{-4}$ and $h_{22} = 50 \times 10^{-6}$. The hybrid representation of a single stage is drawn in Fig. 2.30b.

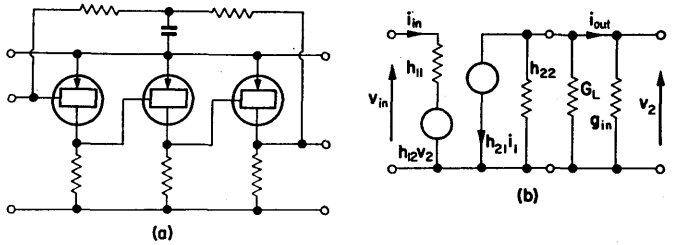



FIG. 2.30. Three-stage d.c. amplifier with an equivalent network of one stage.

Due to the low input resistance $v_2$ is small, and since $h_{12}$ also is small the voltage generator $h_{12}v_2$ may often be neglected for approximate calculations.

The current gain

$$\frac{i_{out}}{i_{in}} = \frac{h_{21} g_{in}}{h_{22} + G_L + g_{in}}. \qquad (2.40)$$

The output voltage

$$v_2 = \beta i_{in} \times \text{shunt resistance}$$

$$= \frac{h_{21}}{h_{22} + G_L + g_{in}} \cdot i_{in}. \qquad (2.41)$$

As $g_{in}$ is very much greater than $G_L$ and $h_{22}$ there is efficient current transfer.

Stage current gain, $a = 40$, so overall current gain $= (40)^3 = 64{,}000$.

Transfer resistance $= v_{out}/i_{in} \doteqdot a^3 \cdot R_L \doteqdot 3{\cdot}5 \times 10^8\ \Omega$.

Voltage gain

$$\frac{Z_t}{r_{in}} \doteqdot \frac{a^3 R_L}{r_{in}} \doteqdot \frac{350 \times 10^6}{1000} \doteqdot 3{\cdot}5 \times 10^5.$$

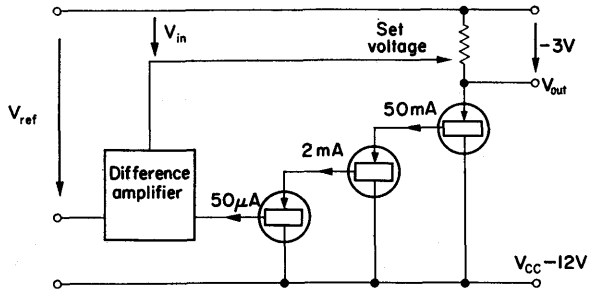



FIG. 2.31. Regulated power supply using a compound common collector stage. The excess voltage $V_{CC} - V_o$ appears across the compound stage.

(b) *Common Collector*

In the stabilized power supply of Fig. 2.31, $V_O$ is to be held constant at $-3$ V for all values of current between 0 and 1 A. The output transistor must therefore be capable of dissipating a maximum power of 9 V × 1 A = 9 W. When drawing 1 A at 3 V the effective load resistance is obviously 3 Ω. This does not appear across the difference amplifier output since the input resistance to the common collector current amplifier,

$$r_{in} \doteqdot 3 \times h_{f1} \times h_{f2} \times h_{f3}.$$

Given that $h_{f1} = 40$, $h_{f2} = 25$ and $h_{f3} = 20$, $r_{in} \doteqdot 60\ \text{k}\Omega$.

The difference amplifier is therefore only lightly loaded by the current amplifier.

(c) *CE–CB–CC d.c. Amplifier* (Fig. 2.32)

The common collector output stage provides a low impedance voltage output. The input resistance of this stage, for $R_E = 5$ kΩ, is $\beta_3 R_E = 200$ kΩ. Thus the effective load presented to the common base transistor is 100 kΩ. Since the current gain of such a stage is unity, its transfer resistance $R_{T2}$ is also 100 kΩ. Current gain provided by stage 1 is approximately equal to $\beta_1$ of $T_1$ since this transistor feeds into the low input resistance of the common base stage. Thus the over-all transfer resistance (output voltage divided by input current),

$$R_T = \beta_1 R_{T2} = 5 \text{ MΩ}.$$

This implies that 1 μA of input current gives rise to an output of 5 V.

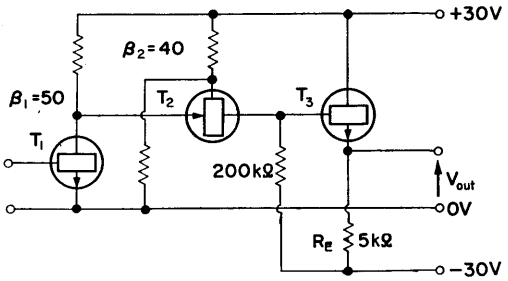



FIG. 2.32. A d.c. amplifier using common emitter, common base and common collector stages in tandem.

## 2.14. SUMMARY OF THE CHARACTERISTICS OF TRANSISTOR AMPLIFIERS IN TERMS OF *r* PARAMETERS

For the three basic configurations of transistor amplifiers, Table 2.2 sets out input and output resistance, and voltage and current gain, in terms of *r* parameters.

In this table the top expressions in each case are exact, while the lower expressions are approximate.

TABLE 2.2

| | Common Base | Common Emitter | Common Collector |
|---|---|---|---|
| $R_{in}$ | $r_e + r_b \dfrac{r_c - r_m + R_L}{r_b + r_c + R_L}$ | $r_b + r_e \dfrac{r_c + R_L}{r_d + r_e + R_L}$ | $r_b + r_c \dfrac{r_e + R_L}{r_d + r_e + R_L}$ |
| | $r_e + r_b(1 - a)$ | $r_b + \dfrac{r_e}{1 - a}$ | $\dfrac{R_L}{1 - a}$ |
| $R_{out}$ | $r_c - r_b \dfrac{r_m - R_g - r_e}{R_g + r_e + r_b}$ | $r_d + r_e \dfrac{R_g + r_b + r_m}{R_g + r_b + r_e}$ | $r_e + r_d \dfrac{R_g + r_b}{R_g + r_b + r_c}$ |
| | $r_c \cdot \dfrac{r_e + r_b(1 - a) + R_g}{r_e + r_b + R_g}$ | $r_d + r_e \dfrac{r_m + R_g}{r_e + r_b + R_g}$ | $r_e + (r_b + R_g)(1 - a)$ |
| $A_v$ | $\dfrac{(r_m + r_b) R_L}{r_b(r_d + r_e + R_L) + r_e(r_c + R_L)}$ | $\dfrac{R_L(r_m - r_e)}{r_b(r_d + r_e + R_L) + r_e(r_c + R_L)}$ | $\dfrac{r_c R_L}{r_b(r_d + r_e + R_L) + r_c(r_e + R_L)}$ |
| | $\dfrac{aR_L}{r_e + r_b(1 - a)}$ | $\dfrac{-aR_L}{r_e + r_b(1 - a)}$ | 1 |
| $A_i$ | $\dfrac{r_m + r_b}{r_b + r_c + R_L}$ | $\dfrac{r_m - r_e}{r_d + r_e + R_L}$ | $\dfrac{r_c}{r_d + r_e + R_L}$ |
| | $a\ (=\alpha)$ | $\dfrac{a}{1 - a}\ (=\beta)$ | $\dfrac{1}{1 - a}\ (=1 + \beta)$ |

CHAPTER 3

# The Capacitively Coupled Amplifier

## Introduction

In applications where an amplifier is not required to operate on very low frequencies (below 1 c/s) transformer or capacitor coupling is used. This isolates the d.c. voltages of an anode (usually of the order of 100 V) from the grid of the following stage.

Transformer coupling is frequently used with tuned amplifiers and in applications where a low resistance is required between the grid and cathode of a valve. Capacitance coupling is very widely used because of its simplicity and cheapness.

## 3.1. Bandwidth

The capacitively coupled amplifier has a finite bandwidth (see Fig. 3.1.) The gain falls off as the reactance of the coupling capacitor increases at low frequency, and also at high frequency due to the shunting effect of the stray capacitance between anode and the earth or common connection.

### *Equivalent Network*

If the valves of Fig. 3.1 are replaced by incremental models, and the cathode bias resistor $R_K$ is bypassed by the capacitor $C_K$, the gain and frequency response can be obtained from the equivalent network of Fig. 3.2.

The capacitance $C_1$ is made up of the valve anode–cathode interelectrode capacitance together with the shunt capacitance

due to the valve holder and wiring. $C_2$ represents the input capacitance of $V_2$ together with the stray wiring capacitance.

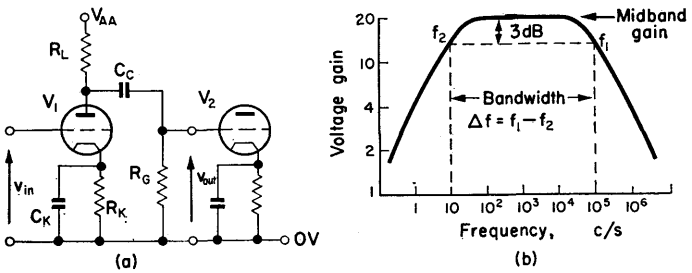



FIG. 3.1. (a) A capacitively coupled amplifier stage. (b) Gain plotted against frequency. The upper and lower bandwidth limits are $f_1$ and $f_2$, i.e. the frequencies at which the gain has fallen to $1/\sqrt{2}$ of the midband value.

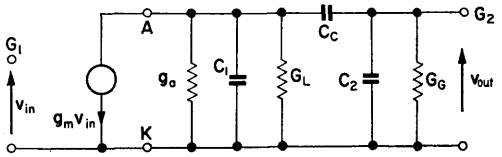



FIG. 3.2. Incremental representation of the amplifier of Fig. 3.1, neglecting $C_K$ and $R_K$. $C_1$ and $C_2$ are shunt capacitances.

## 3.2. DETERMINATION OF GAIN AND FREQUENCY RESPONSE

### *Midband Gain*

The gain of an amplifier is determined at midband frequency where $C_C$, $C_1$ and $C_2$ can be neglected:

$$\text{midband gain} = v_{out}/v_{in} = A_0 = -g_m R, \qquad (3.1)$$

where

$$R = \frac{1}{G} = \frac{1}{g_a + G_L + G_G}.$$

This is apparent from inspection of Fig. 3.3 since $v_{out}$ is produced by the current $g_m v_{in}$ flowing through $g_a$, $G_L$ and $G_G$ in parallel.

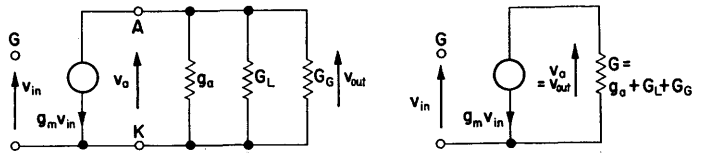



FIG. 3.3. Midband equivalent network of the circuit of Fig. 3.1.

$$\text{Gain} = A_0 = g_m R.$$

*High Frequency Gain*

As the operating frequency of the amplifier is increased, the reactance of the shunt capacitance between anode and earth, $1/\omega(C_1 + C_2)$ in Fig. 3.2, decreases. When this approaches $R$ in value it can no longer be neglected. Hence the high frequency equivalent network of Fig. 3.4. The output voltage is developed by the generator current, $g_m v_{in}$, flowing in $G$ and $C_S$ in parallel:

$$A_1(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{-g_m}{G + sC_s} = \frac{-g_m}{G} \frac{1}{1 + sC_s/G},$$

$$= A_0 \frac{1}{1 + sT_1} \left( \text{where } T_1 = \frac{C_s}{G} = C_s R \right). \qquad (3.2)$$

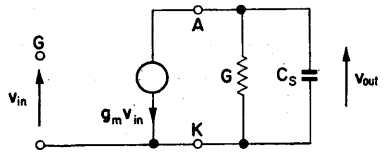



FIG. 3.4. High frequency equivalent network. High frequency gain,

$$A_1(j\omega) = A_0 \frac{1}{1 + j\omega T_1}, \text{ where } T_1 = C_S R.$$

As shunt capacitance is always present, the gain will always fall off at high frequencies.

*High Frequency Response*

The frequency response can be obtained by substituting $j\omega$ for $s$ in eqn. (3.2):

$$A_1(j\omega) = A_0 \frac{1}{1 + j\omega T_1},$$

and, rationalizing,

$$A_1(j\omega) = \frac{1}{1 + (\omega T_1)^2}(1 - j\omega T_1),$$

$$= |A_1(j\omega)| \measuredangle \theta_1,$$

where $$|A_1(j\omega)| = \frac{A_0}{\sqrt{[1 + (\omega T_1)^2]}}, \tag{3.3}$$

and $$\theta_1 = -\tan^{-1} \omega T_1.$$

At very high frequencies, i.e. frequencies at which $\omega \gg 1/T_1$ (and consequently $\omega T_1 \gg 1$), the real part of the gain expression

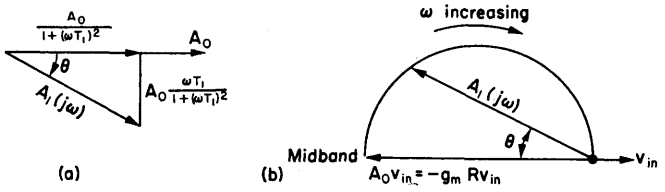



FIG. 3.5. (a) Resolved components of high frequency gain. (b) Polar diagram of output voltage as a function of $\omega$. As $\omega$ becomes very large $\theta$ tends to 90°.

is very small and $A_1(j\omega)$ tends to $-j(A_0/\omega T_1)$. This implies that the phase is retarded 90° on the midband value, and gain falls inversely with frequency. The locus of the gain lies on the circumference of a semicircle with midband gain as diameter (Fig. 3.5b)

*Bandwidth Limit*

The upper bandwidth limit is the frequency at which the gain falls to $1/\sqrt{2}$ of the midband value $A_0$. From eqn. (3.3), the upper bandwidth frequency $\omega_1 = 1/T_1$, since

$$|A_1(j\omega_1)| = \frac{A_0}{\sqrt{(1+1)}} = \frac{A_0}{\sqrt{2}}.$$

The angle of the phasor relative to $A_0$,

$$\theta_1 = -\tan^{-1}\omega T_1 = -\tan^{-1} 1 = -45° \quad \text{(see Fig. 3.6)}.$$

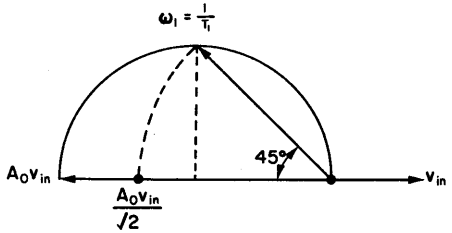



FIG. 3.6. Phasor for $\omega_1 = 1/T_1$. $\omega_1$ is the radian frequency at which $A$ falls to $A_0/\sqrt{2}$.

EXAMPLE. Valve EF86. This is a pentode with $r_a$ greater than 1 MΩ. When used with an anode load resistance of 100 kΩ the measured gain is −150. (The negative sign indicates signal inversion.)

The midband gain $A_0 = -g_m R$, where $R$ in this case is approximately 100 kΩ (i.e. $R_L$). Thus,

$$g_m = \frac{150}{100 \times 10^3} = 1{\cdot}5 \text{ mA/V}.$$

By measuring the upper bandwidth point $f_1 = \omega_1/2\pi$, the shunt capacitance can be determined. For $f_1$ of 80 kc/s, and

allowing 11·5 pF for the oscilloscope probe,

$$\omega_1 = \frac{1}{T_1} = 2\pi \times 80 \times 10^3,$$

$$C_s = \frac{1}{\omega_1 R} = \frac{1}{2\pi \times 8 \times 10^9} = 20 \text{ pF}.$$

Thus, the valve output capacitance $C_{ak}$ and wiring capacitance equals $20 - 11{\cdot}5 = 8{\cdot}5$ pF.

## 3.3. Estimation of Frequency Response using Straight Line Asymptotes[13]

The magnitude of the gain is given by eqn. (3.3),

$$|A_1(j\omega)| = \frac{A_0}{\sqrt{[1 + (\omega T_1)^2]}}.$$

At frequencies where $\omega T_1$ is very much greater than unity

$$|A_1(j\omega)| \doteqdot \frac{A_0}{\omega T_1}.$$

The gain falls as $\omega$ increases. If the amplitude of the gain at frequency $\omega_a$ is $A_a$, then at frequency $2\omega_a$ the gain will be $A_a/2$.

Doubling the frequency is an octave change and thus the gain is halved for each octave. By similar reasoning, a decade increase in frequency reduces the gain by a tenth. As shown in Fig. 3.1 it is usual to employ logarithmic axes so that at frequencies $\omega \gg 1/T_1$ the gain curve is a straight line:

$$20 \log \left| \frac{A_1(j\omega_a)}{A_2(j2\omega_a)} \right| = 20 \log_{10} \frac{A_a}{A_a/2} = 20 \log 2 = 6 \text{ dB}.$$

That is, the gain falls at a rate of 6 dB/octave, or 20 dB/decade. The straight line representing $|A_1(j\omega)| \doteqdot A_0/T_1$ is shown in Fig. 3.7. If the line is projected back so that it meets the midband gain line, it will do so at $\omega_1 = 1/T_1$.

In the previous section it was shown that at $\omega_1$ the gain had fallen from $A_0$ to $A_0/\sqrt{2}$, a fall of 3 dB, since $20 \log_{10} \sqrt{2} = 3$. The error in taking the straight line approximation of the amplitude response is shown in Fig. 3.7 to be a maximum of +3 dB at $\omega_1$ falling to +1 dB at $\omega_1/2$ and $2\omega_1$.

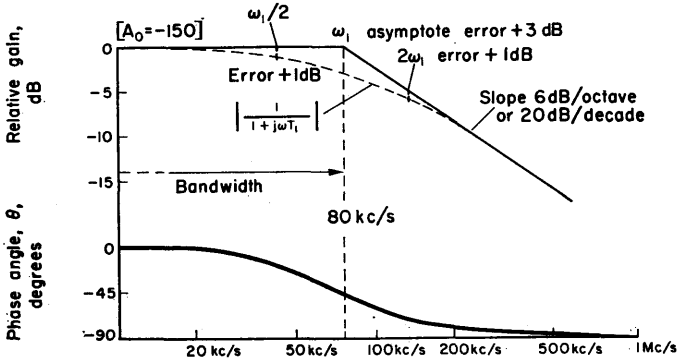



FIG. 3.7. Frequency response using straight line asymptotes. Gain is relative to midband. Straight line approximation is made by projecting down from $\omega_1$ ($= f_1/2\pi$) on the 0 dB axis, at a slope of 20 dB/decade. Note that the ordinate is gain relative to $A_0$.

It is convenient to draw the amplitude response relative to the gain $A_0$. A negative sign shows that the gain is less than $A_0$ and the bandwidth is given by the frequencies at which the relative gain is −3 dB:

$$\text{relative gain} = -20 \log_{10} \left| \frac{A_0}{A(j\omega)} \right|.$$

The straight line approximation for $A = |A_0/(1 + j\omega T_1)|$ can be drawn by projecting down from $\omega_1$ on the zero relative gain line at a slope of 6 dB for each octave of frequency. Often it is more convenient to use the slope of 20 dB/decade as the relative gain axis is usually calibrated in tens and the logarithmic frequency scales repeat in cycles of ten.

Consider the example:

$$R = 100\,\text{k}\Omega, \quad C_s = 20\,\text{pF}.$$

$$T_1 = C_s R = 2 \times 10^{-6}\ \text{sec}.$$

$$\omega_1 = \frac{1}{T_1} = 5 \times 10^5\ \text{r/s}.$$

$$f_1 = \frac{\omega_1}{2\pi} = 79{\cdot}6\ \text{kc/s}.$$

From $f_1$ the asymptote is drawn with a slope of 6 dB/octave.

## 3.4. Gain-bandwidth Product

The lower bandwidth point of an amplifier can be reduced in frequency by increasing the coupling capacitor, and can be eliminated by direct coupling the stage. (See Chapter 6.)

The high frequency bandwidth point is largely a function of the valve and its value can be considered to be the bandwidth as far as the valve is concerned. This is shown in Fig. 3.8.

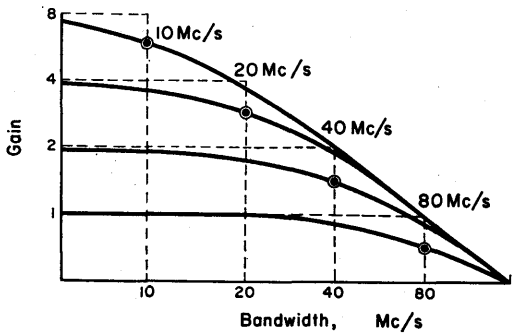



FIG. 3.8. Gain plotted against bandwidth for a gain-bandwidth product of 80 Mc/s. If a gain of 80 Mc/s is required, the gain is unity.

Thus the bandwidth, in radian frequency,

$$\omega_1 = \frac{1}{T_1} = \frac{1}{C_s R} \text{ r/s.} \tag{3.4}$$

$C_s$ is the total shunt capacitance of an amplifying stage and will in general be made up of the valve input and output capacitances, together with the wiring capacitance. $R$ is the total shunt resistance as in Figs. 3.1a and 3.3.

As the gain of an amplifier is $A_0 = g_m R$ [eqn. (3.1)],

$$\text{gain} \times \text{bandwidth}, \quad A_0\omega_1 = g_m R \times \frac{1}{C_s R} = \frac{g_m}{C_s} \text{ r/s.}$$

Thus,

$$\text{gain-bandwidth product} = \frac{g_m}{2\pi C_s} \text{ c/s,} \tag{3.5}$$

which is independent of the effective load resistance $R$.

This implies that once a valve has been specified the gain-bandwidth product is fixed. For a given gain there will be a resulting bandwidth of

$$f_1 = \frac{g_m}{2\pi C_s} \times \frac{1}{A_0} \text{ c/s.}$$

EXAMPLES. Consider a valve with $g_m = 10$ mA/V, and $C_s = C_{in} + C_{out} = 20$ pF:

$$\text{gain} \times \text{bandwidth} = \frac{10 \times 10^{-3}}{2\pi \times 20 \times 10^{-12}} = 80 \text{ Mc/s.}$$

If a gain of 10 is required, the bandwidth will be 8 Mc/s. For an amplifier with 80 Mc/s bandwidth, the gain is unity. Thus for wideband amplifiers, the $g_m$ should be as large as possible and $C_s$ as small as possible.

The $g_m$ is usually increased by reducing the grid–cathode spacing, which can be made very small with modern " frame-grid" construction. This unavoidably increases the input capacitance.

Present- day wideband amplifying valves have $g_m = 50$ mA/V and gain-bandwidth product in the region of 250 Mc/s.

*Reduction in Gain-bandwidth Product with Large Anode Resistors*

Although the curves of Fig. 3.8 are theoretically correct, in practice a large anode load resistor will mean that the valve will be run at a lower current than for a smaller resistor. This is because it is awkward to have an anode supply higher than about 300 V. The lower current means a lower $g_m$ and, consequently, a smaller gain-bandwidth product at high stage gains.

## 3.5. Low Frequency Gain

As the frequency of $v_{in}$ in Fig. 3.1a is reduced, the reactance of the coupling capacitance $1/\omega C_C$ increases and is no longer negligible compared with $R_G$. The output voltage $v_{out}$ is no longer equal to $v_a$, the anode voltage, but tends to zero as $\omega$ tends to zero.

This is shown in the amplitude response of Fig. 3.1b.

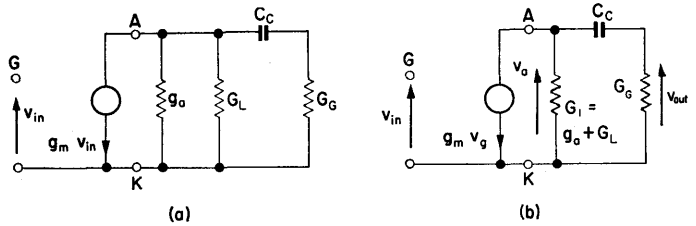



FIG. 3.9. Low frequency equivalent network. The shunt capacitance $C_s$ in Fig. 3.4 is ignored since its effect is negligible at low frequency.

At low frequency it is possible to neglect the shunt capacitance, because its small value and the low frequency combine to produce a reactance that is much greater than the effective resistance $R$.

Figure 3.9 is a valid equivalent network at low frequency provided $C_K$ is still effectively bypassing $R_K$.

The nodal equations for Fig. 3.9b (see Appendix A) are

$$(G_1 + sC_C)\, v_a - sC_C v_{\text{out}} = -g_m v_g,$$

$$-sC_C v_a + (G_G + sC_C)\, v_{\text{out}} = 0,$$

where $v_a$ is the anode voltage, $v_{\text{out}}$ is the output voltage and $v_g$ is the grid voltage ($= v_{\text{in}}$).

The gain expression, $A_2(s)$, is now a function of $s$ ($= j\omega$ for sin usoidal inputs):

$$A_2(s) = \frac{v_{\text{out}}(s)}{v_{\text{in}}(s)} = \frac{-g_m sC_C}{(G_1 + sC_C)(G_G + sC_C) - (sC_C)^2}$$

$$= \frac{-g_m}{G_1 + G_G + (G_1 G_G / sC_C)}.$$

Removing the factor $G_1 + G_G = g_a + G_L + G_G = G$,

$$A_2(s) = \frac{-g_m}{G_1 + G_G} \cdot \frac{1}{1 + [G_1 G_G / sC_C(G_1 + G_G)]}$$

$$= A_0 \frac{1}{1 + [(g_a + G_L)\, G_G / sC_C(g_a + G_L + G_G)]}.$$

$$\text{since } A_0 = \frac{-g_m}{G_1 + G_G}.$$

Therefore

$$A_2(s) = A_0 \frac{1}{1 + (1/sT_2)}, \tag{3.6}$$

where $T_2 = C_C R$, and

$$R = \frac{g_a + G_L + G_G}{(g_a + G_L)\, G_G} = \frac{r_a R_L}{r_a + R_L} + R_G.$$

If

$$R_G \gg \frac{r_a R_L}{r_a + R_L}, \quad T_2 = C_C R_G.$$

*Low Frequency Response*

The frequency response can be obtained by substituting $j\omega$ for $s$:

$$A_2(j\omega) = A_0 \frac{1}{1 + (1/j\omega T_2)} = \frac{A_0}{1 + (1/\omega T_2)^2} \cdot \left(1 - \frac{1}{j\omega T_2}\right)$$

$$= |A_2(j\omega)| \measuredangle \theta, \tag{3.7}$$

where

$$|A_2(j\omega)| = \frac{A_0}{\sqrt{[1 + (1/\omega T_2)^2]}},$$

and

$$\theta_2 = \tan^{-1} \frac{1}{\omega T_2}.$$

At very low frequencies (i.e. frequencies at which $\omega \ll 1/T_2$ and consequently $\omega T_2 \ll 1$) the real part of the gain expression is very small and $A(j\omega)$ tends to $jA_0\omega T_2$, implying that the phase is advanced 90° on the midband value and the gain falls directly with frequency. The locus of the gain lies on the circumference of a semicircle with the midband gain as diameter (Fig. 3.10).

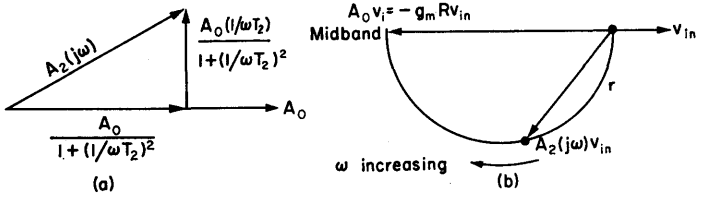



FIG. 3.10. (a) Resolved components of low frequency gain. (b) Polar diagram of output voltage as a function of $\omega$.

*Estimation of Frequency Response*

This can be done in a similar manner to the high frequency case.

EXAMPLE. Consider the second valve of Fig. 3.1a neglecting (for the present) the cathode network:

$$r_a = 17\ \text{k}\Omega, \quad R_L = 25\ \text{k}\Omega, \quad R_G = 150\ \text{k}\Omega, \quad C_C = 0{\cdot}1\ \mu\text{F}$$

and

$$g_m = 2 \text{ mA/V}.$$

From eqn. (3.6),

$$R = \frac{r_a R_L}{r_a + R_L} + R_G = 160 \text{ k}\Omega.$$

$$T_2 = C_C R = 0{\cdot}016 \text{ sec}.$$

$$\omega_2 = 1/T_2 = 62{\cdot}5 \text{ r/s}.$$

$$f_2 = \omega_2/2\pi = 9{\cdot}98 \text{ c/s}.$$

The breakpoint for the approximate curve is the 3 dB frequency, $f_2 \doteqdot 10$ c/s, and the asymptote is drawn from this point with a slope of 6 dB/octave.

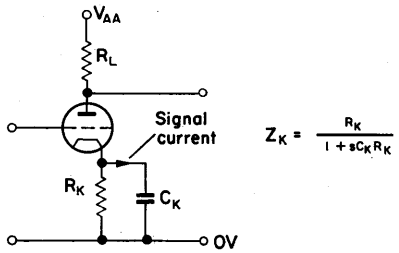



FIG. 3.11. Triode amplifier with cathode bias and bypass capacitor.

## 3.6. EFFECT OF CATHODE BYPASS CAPACITOR ON FREQUENCY RESPONSE

The gain of the network of Fig. 3.11 is

$$A = \frac{-\mu R_L}{r_a + R_L + (\mu + 1) Z_K}$$

from eqn. (1.12). Substituting

$$Z_K = \frac{R_K}{1 + sT_K},$$

where $T_K = C_K R_K$,

$$A(s) = \frac{-\mu R_L}{r_a + R_L + (\mu + 1) R_K} \times$$

$$\times \frac{1 + sT_K}{1 + \{sT_K(r_a + R_L)/[r_a + R_L + (\mu + 1) R_K]\}},$$

or

$$A(s) = A_K \cdot \frac{1 + sT_K}{1 + sT'_K}, \tag{3.8}$$

where

$$A_K = \frac{-\mu R_L}{r_a + R_L + (\mu + 1) R_K},$$

and

$$T'_K = T_K \cdot \frac{r_a + R_L}{r_a + R_L + (\mu + 1) R_K}.$$

At operating frequencies $C_K$ bypasses the cathode resistor as its impedance is very much less than $R_K$, and the gain is

$$A_0 = \frac{-\mu R_L}{r_a + R_L} \quad (= -g_m R).$$

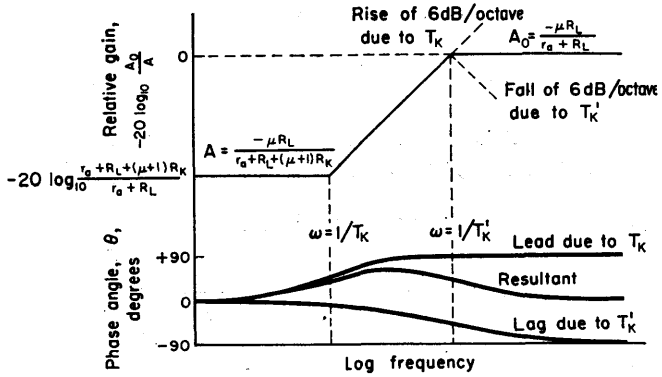



FIG. 3.12. Straight line approximation of eqn. (3.8). Effect of cathode bypass capacitor at low frequency. At midband the bias network has no effect on the frequency response.

At very low frequencies $C_K$ becomes less effective and

$$A(s) = \frac{-\mu R_L}{r_a + R_L + (\mu + 1) R_K}.$$

$C_K$ must be made large enough to ensure that it is effective in bypassing $R_K$ in the required operating frequency band.

The frequency response is of the form of Fig. 3.12 and can be obtained by applying the methods of § 3.3.

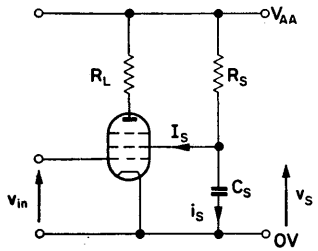



FIG. 3.13. Pentode with screen grid decoupling. Signal currents are passed to earth through the decoupling capacitor $C_s$.

## 3.7. EFFECT OF SCREEN DECOUPLING ON FREQUENCY RESPONSE

When the screen grid current is supplied from a series resistor, as described in § 1.7, gain will be very much reduced unless the impedance of the screen network is made negligible by a decoupling capacitor. Such a network is shown in Fig. 3.13.

### *Screen Grid Degeneration*

The signal voltage developed at the screen grid is

$$v_s = \frac{-\mu_s Z_S}{r_s + Z_S} v_{in}, \tag{3.9}$$

since the screen acts in a manner similar to the anode of a triode. If the screen is fully decoupled the voltage $v_s$ is zero, as $Z_S$ is effectively zero.

As the signal frequency is reduced the impedance of $C_S$ will increase and at zero frequency $Z_S$, which is $R_S$ in parallel with $C_S$, becomes $R_S$.

If the screen voltage varies, the signal voltage at the anode is less than it would be if the screen were held constant.

If $v_{in}$ is positive-going, $v_s$ will fall, if not decoupled, reducing the $g_m$ and consequently reducing the anode voltage change.

The simplest method of assessing the effect of the screen grid is to use eqn. (3.9) and refer the effect of $v_s$ back to the control grid.

$$\mu_s = \left[\frac{\delta V_S}{\delta V_{in}}\right] \quad (I_S \text{ constant}), \tag{3.10}$$

$$r_S = \left[\frac{\delta V_S}{\delta I_S}\right] \quad (V_{in} \text{ constant}), \tag{3.11}$$

$$Z_S(s) = \frac{R_S}{1 + sC_SR_S}. \tag{3.12}$$

These parameters are defined in the same manner as $\mu$ and $r_a$. The anode voltage has only a second order effect on their values.

The voltage at the screen grid can be referred to the control grid by dividing $v_s$ by $\mu_s$.

Thus $v_{in} + v_s/\mu_s$ is the effective control grid voltage, and

$$v_{in}\,(\text{effective}) = v_{in}\left(1 - \frac{Z_S}{r_s + Z_S}\right) = v_{in}\frac{r_s}{r_s + Z_S}. \tag{3.13}$$

The voltage gain,

$$A(s) = A_0\frac{r_s}{r_s + Z_S} \quad [\text{where } A_0 \text{ is the midband gain, see eqn. (3.1)}],$$

$$= A_0\frac{r_s}{r_s + R_S}\cdot\frac{1 + sC_SR_S}{1 + [sC_SR_Sr_s/(R_S + r_s)]}, \tag{3.14}$$

$$= A_S\frac{1 + sT_S}{1 + sT'_S}, \tag{3.15}$$

where

$$A_S = A_0 \frac{r_s}{r_s + R_S},$$

$$\left.\begin{aligned} T_S &= C_S R_S \\ T_S' &= T_S \frac{r_s}{R_S + r_s} \end{aligned}\right\} T_S > T_S'.$$

EXAMPLE. Referring to Fig. 3.13, let the valve be an EF86, $R_L = 100\ \text{k}\Omega$, $R_S = 390\ \text{k}\Omega$, $C_S = 0{\cdot}002\ \mu\text{F}$ and $V_S = 110\ \text{V}$. The measured values of $r_s$ and $\mu_s$ are 110 kΩ and 40 respectively.

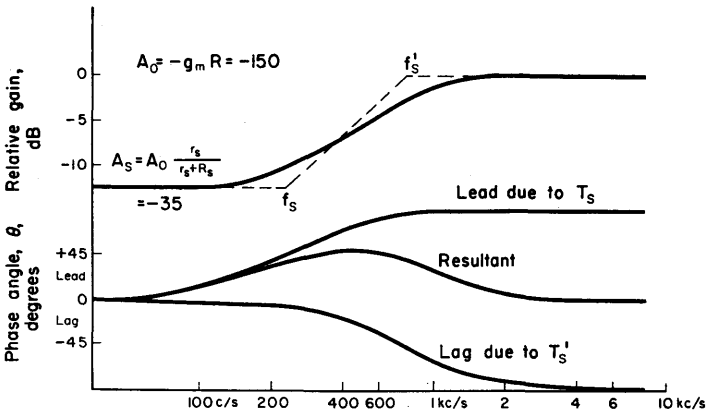



FIG. 3.14. Measured and calculated response for partially decoupled screen grid. Maximum phase shift is 60° at $f = \sqrt{(f_s f_s')}$. The straight line approximation is drawn by joining $f_s$ on the $A$ line to $f_s'$ on the $A_3$ line.

Voltage gain, with screen decoupled, $A_0 = -150$.
Voltage gain, for $\omega C_S = 0$, $A_S = -35$.

$$T_S = C_S R_S = 7{\cdot}8 \times 10^{-4}\ \text{sec},$$

$$T_S' = T_S \frac{r_s}{r_s + R_S} = 1{\cdot}7 \times 10^{-4}\ \text{sec}.$$

Therefore $\omega_S = 1280$ r/s, $\omega'_S = 5800$ r/s,

and $f_S = 260$ c/s, $f'_S = 920$ c/s.

The frequency response of this example is plotted in Fig. 3.14.

## 3.8. Anode Decoupling (Fig. 3.15)

Anode decoupling can be used to eliminate signal currents from the power supply of a network. It will also reduce the possibility of signals entering a network from the power supply leads. In

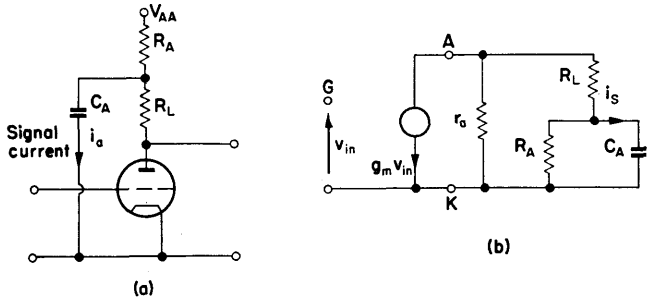



FIG. 3.15. Circuit to show anode decoupling, and its equivalent network.

multistage systems, the power supply forms a common impedance and, unless this is very low (as it is with most voltage stabilized supplies), the coupling due to this element can cause oscillation. The frequency of oscillation will be that at which the low frequency phase shifts provide an over-all phase shift of 360°, thus causing positive feedback. This low frequency oscillation is called "motor-boating". All power supplies tend to have a low impedance at high frequency because of the shunt capacitor of the output filter.

The gain of the network of Fig. 3.15b is

$$A = \frac{-\mu(R_L + Z_A)}{r_a + R_L + Z_A},$$

where

$$Z_A = \frac{R_A}{1 + sC_AR_A}$$

(i.e. $R_A$ and $C_A$ in parallel). Thus

$$A(s) = \frac{-\mu R_L}{r_a + R_L} \cdot \frac{1 + [R_A/R_L(1 + sC_AR_A)]}{1 + [R_A/(r_a + R_L)(1 + sC_AR_A)]} \tag{3.16}$$

$$= A_0 \frac{1 + sC_AR_A + (R_A/R_L)}{1 + sC_AR_A + [R_A/(r_a + R_L)]} \tag{3.17}$$

$$= A_0 \frac{1 + (R_A/R_L)}{1 + [R_A/(r_a + R_L)]} \times$$

$$\times \frac{1 + [sC_AR_AR_L/(R_A + R_L)]}{1 + [sC_A(r_a + R_L)\,R_A/(R_A + R_L + r_a)]} \tag{3.18}$$

$$= A_A \frac{1 + sT_A}{1 + sT'_A}, \quad \text{where} \quad A_A = A_0 \frac{1 + (R_A/R_L)}{1 + [R_A/(r_a + R_L)]}, \tag{3.19}$$

$$T_A = \frac{C_AR_AR_L}{r_a + R_L} \quad \text{and} \quad T'_A = \frac{C_A(r_a + R_L)\,R_A}{R_A + R_L + r_a}$$

(i.e. $T'_A > T_A$).

EXAMPLE. Anode decoupling is required to reduce any 50 c/s component of the power supply by 100 (i.e. 40 dB).

As $f$ becomes very large the alternating voltage at the anode, due to the power supply, is proportional to $v_r/j\omega C_AR_A$, where $v_r$ is the ripple voltage.

The attenuation of a simple lag is 20 dB/decade (§ 3.3). To reduce 50 c/s ripple by 40 dB it is necessary to introduce a break-point two decades below 50 c/s, i.e. at $\frac{50}{100}$ c/s. Therefore

$$\omega_A = \frac{1}{C_AR_A} = \frac{2\pi \times 50}{100} = 3{\cdot}14,$$

which yields $C = 2\mu$, $R \doteqdot 150\ \text{k}\Omega$.

This network will cause the gain of the amplifier to increase at low frequencies and will give a phase lag (see Fig. 3.16).

Thus it is possible for anode decoupling to be used to extend the low frequency bandwidth by making $f_A$ coincide with the 3 dB point of the coupling network.

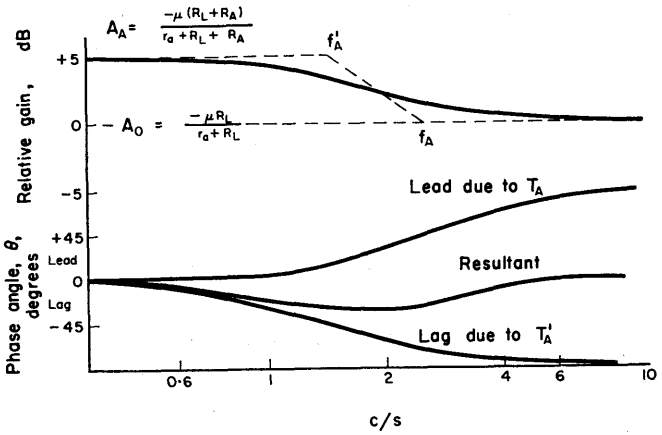



FIG. 3.16. Phase lag due to anode decoupling for a valve with $\mu = 100$, $r_a = 100$, $R_L = 50\,k\Omega$, $R_A = 150\,k\Omega$ and $C_A = 2\,\mu F$. Note the increase in gain at low frequency.

## 3.9. AMPLIFIER TIME RESPONSE[3]

Complementary to the frequency response of a network is its behaviour to a step input. This is the *time response*, as the amplitude of the output signal varies with time.

The expressions obtained as functions of the complex variable $s$ can be transformed into functions of time as follows.

### *Effect of Shunt Capacitance* (see Fig. 3.4)

When a step of voltage is applied to the input of an amplifier, the output voltage can rise only as $C_S$ is charged. Thus,

for a fast rise, the time constant $C_S R$ must be as small as possible.

$$v_{out}(s) = \frac{A_0}{(1 + sT_1)} v_{in}(s) \quad \text{[from eqn. (3.2)]}$$

$$= \frac{A_0}{T_1} \cdot \frac{1}{s(s + 1/T_1)} \quad \text{(for unit step input).}$$

Thus

$$v_{out}(t) = A_0[1 - \exp(-t/T_1)] \quad \text{(from transform pair No. 3).} \tag{3.20}$$

This expression is shown in Fig. 3.17.

Initial slope of response at $t = 0$ is

$$\frac{\mathrm{d}}{\mathrm{d}t} v_{out}(t_0) = \frac{g_m}{C_s}, \tag{3.21}$$

which is identical with the gain-bandwidth product [eqn. (3.5)].

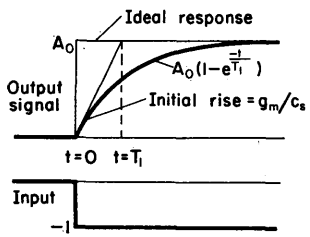



FIG. 3.17. Response to a negative step input showing the effect of shunt capacitance on performance.

*Effect of Coupling Capacitance* (see Fig. 3.9)

When a step function is applied to the coupling capacitor the full value appears at the grid terminal. As the capacitor charges, this voltage falls to zero on a time constant $T_2 = C_C R$, as shown in Fig. 3.18:

$$v_{out}(s) = \frac{A_0}{1 + (1/sT_2)} v_{in}(s) \quad \text{[from eqn. (3.6)].}$$

For a negative step function input,

$$v_{out}(t) = A_0 \exp(-t/T_2) \tag{3.22}$$

(from transform pair No. 2).

In most applications $T_2$ will be much greater than the length of any pulse $\tau$ that constitutes the input signal. The top of the

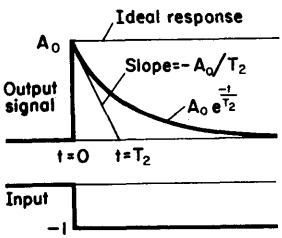



FIG. 3.18. Time response to a step input showing the effect of coupling capacitance.

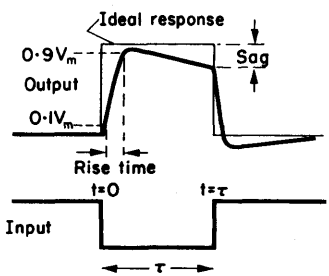



FIG. 3.19. Pulse response showing the effect of $C_S$ and $C_C$. Rise time is the time the waveform takes to rise from 0·1 to 0·9 of its final value.

pulse falls linearly with time and the slope is proportional to $1/T_2$. If $C$ is infinite (or the amplifier is direct coupled) the slope will be zero. The fall in output amplitude is called "sag".

*Combined Effects of Coupling and Shunt Capacitance*

If the high frequency performance is inadequate, the rise time will be excessive, while large sag indicates poor low frequency performance (see Fig. 3.19):

$$\text{Rise time} \doteqdot 2{\cdot}2\, R_L C_s. \tag{3.23}$$

$$\text{Percentage sag} \doteqdot \frac{\tau}{C_C R_G} \cdot 100. \tag{3.24}$$

## 3.10. Tandem Stages

As straight line asymptotes are in logarithmic form, they can be added arithmetically. An example is given in Chapter 6.

## 3.11. Triode Amplifier

### Design Example 3.1

Required, a capacitively coupled amplifier having a voltage gain of 10. A 300 V supply is available. Let the valve chosen be a 12 AU7 whose characteristics are plotted in Fig. 3.20. If a load line for $R_L = 20\,\text{k}\Omega$ is constructed, it is obvious that the required gain can be achieved.

If the operating bias is chosen as $-5$ V,

$$R_K = \frac{-V_{GK}}{I_A} = \frac{5\,\text{V}}{7\,\text{mA}}$$

$$= 714\,\Omega \quad (\text{a } 680\,\Omega \text{ resistor is suitable}).$$

*High frequency response.* The upper 3 dB point is given by $\omega_1 = 1/T_1$, where $T_1 = G/C$ and $G = g_a + G_L$.

The output capacitance of the valve is nominally 0·5 pF. Wiring capacitance will raise the value of $C$ to 18 pF. The $r_a$ can

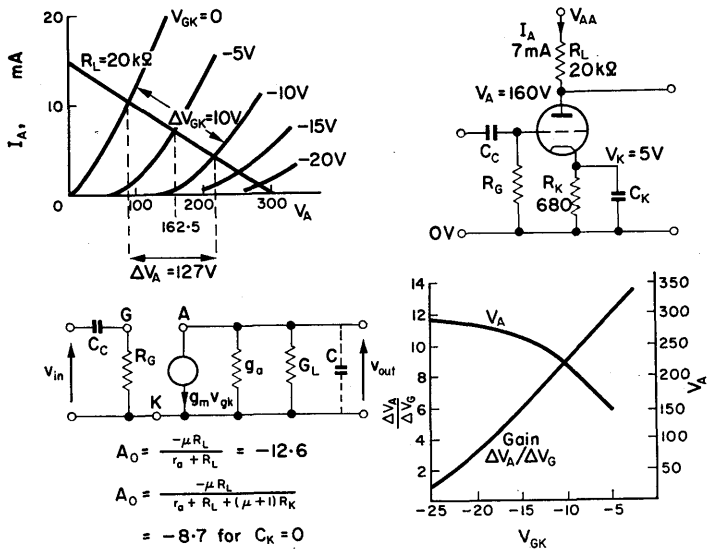



FIG. 3.20. The triode as a voltage amplifier.

be measured from the characteristic at the operating point and is 8·5 kΩ.

$$G = g_a + G_L = \frac{10^{-3}}{8·5} + \frac{10^{-3}}{20} = \frac{10^{-3}}{6},$$

or $R = 6\ \text{k}\Omega$.

$$T_1 = C_s R = 18\ \text{pF} \times 6\ \text{k}\Omega = 108 \times 10^{-9}\ \text{sec}.$$

$$\omega_1 = \frac{1}{T_1} = 9·26 \times 10^6\ \text{r/s}.$$

$$f_1 = \frac{\omega_1}{2\pi} = 1·47\ \text{Mc/s}.$$

If this frequency is too high, $C_s$ can be increased by introducing a capacitor between the anode and the common line. Increasing $R_L$ will decrease the bandwidth, but increases the gain as the gain-bandwidth product is constant.

*Low frequency response.*

(a) *Coupling capacitor and grid leak.* If the input signal is supplied from a low impedance source the time constant $T_2 = C_C R_G$.

For the gain to be down by 3 dB at $f = 100$ c/s,

$$\omega_2 = 680 \text{ r/s} \quad \text{and} \quad T_2 = \frac{1}{680} \text{ sec.}$$

$$R_G = \frac{10^6}{680 \times 0{\cdot}01}\ \Omega \quad (\text{for } C_C = 0{\cdot}01\ \mu) = 147\ \text{k}\Omega.$$

Let

$$R_G = 150\ \text{k}\Omega.$$

(b) *Cathode bypass capacitor.* If the cathode resistor is not bypassed the amplifier gain is

$$A = \frac{-\mu R_L}{r_a + R_L + (\mu + 1) R_K} \quad \text{[from eqn. (1.12)]}$$

$$= -8{\cdot}7 \quad \text{which is below the specification.}$$

To eliminate the reduction in gain due to negative feedback at signal frequencies, $C_K$ must be large enough not to introduce a breakpoint above 25 c/s.

The high frequency breakpoint due to the cathode impedance is given by

$$\omega = \frac{1}{C_K R_K \{(r_a + R_L)/[r_a + R_L + (\mu + 1) R_K]\}} \quad \text{(from § 3.6)}$$

$$= \frac{1}{C_K R_K \times 0{\cdot}69}.$$

For

$$\omega = 157 \text{ r/s} \quad (f = 25 \text{ c/s}), \quad R_K = 680\ \Omega,$$

and

$$C_K = \frac{1}{157 \times 680 \times 0{\cdot}69} = \frac{10^{-5}}{0{\cdot}736} = 13{\cdot}5\ \mu\text{F}.$$

A suitable value would be $C_K = 20\ \mu$F, 6 V working.

## 3.12. Pentode Amplifier

Because of its much greater amplification factor $\mu$, it is possible by using a pentode to obtain much larger gain from a single amplifying stage than with a triode. The maximum gain possible from a valve is the amplification factor. This value of voltage

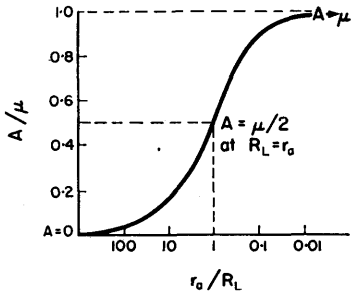



Fig. 3.21. Normalized gain as a function of normalized $r_a$ for $\mu = 50$, $r_a = 10\,\text{k}\Omega$ and $R_L = 100\,\text{k}\Omega$. $r_a/R_L = 0{\cdot}1$, $A/\mu = 0{\cdot}91$ or $A = 45{\cdot}5$.

amplification is approached when the load resistance tends to infinity as shown in Fig. 3.21.

Gain

$$A = \frac{-\mu R_L}{r_a + R_L} \qquad (1.11\text{b})$$

$$= \frac{-\mu}{(r_a/R_L + 1)}$$

$$\doteqdot -\mu \quad \text{for} \quad R_L \gg r_a.$$

For small anode currents $\mu$ is reduced and $r_a$ increases as shown in Fig. 1.12.

DESIGN EXAMPLE 3.2 (Fig. 3.22)

Required, an amplifier with nominal voltage gain of 150 and having signal inversion. The bandwidth must extend from 100 c/s to a minimum of 50 kc/s. A 300 V supply is available.

Such a performance can be readily obtained from a 6AU6 r.f. pentode. However, the characteristics usually supplied by the manufacturer relate to the valve being operated as an r.f. amplifier with large anode current, so as to obtain the maximum gain-bandwidth product.

If the correct conditions for low current operation are required, they can be obtained by the method described in Design Example 6.2.

Rather than determining operation over a wide range of conditions, it is possible to estimate various component values and test the network, modifying any components that cause incorrect operation.

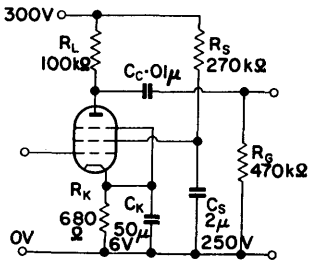



FIG. 3.22. Pentode voltage amplifier.

*Anode voltage* $V_A$. An anode operating voltage of 100 V is reasonable for operation of such an amplifier. This is a compromise between maximum anode voltage swing and non-linearity in the low current region.

*Estimation of* $g_m$. As relatively low current operation is required to obtain the voltage gain, the value of $g_m$ will be considerably less than the nominal figure of 4·5 mA/V. Let an estimated figure be 2 mA/V.

*Load resistor* $R_L$. Gain $A = g_m R_L$ for $R_L \ll r_a$. Thus

$$R_L \doteqdot \frac{160}{2\text{ mA/V}} \doteqdot 80\text{ k}\Omega.$$

A value of $R_L = 100\text{ k}\Omega$ will ensure that the required gain of 150 is obtained, when $r_a$ and $R_G$ are taken into consideration.

*Anode current* $I_A$. The estimated standing anode current,

$$I_A = \frac{V_{AA} - V_A}{R_L} = \frac{200\text{ V}}{100\text{ k}\Omega} = 2\text{ mA}.$$

*Screen current* $I_S$. From the manufacturer's data,

$$I_S \doteqdot 0{\cdot}4\, I_A = 0{\cdot}8\text{ mA}.$$

*Screen voltage* $V_S$. A reasonable value is $V_S = 100\text{ V}$.

*Screen resistor* $R_S$.

$$R_S = \frac{V_{AA} - V_S}{I_S} = \frac{300 - 100\text{ V}}{0{\cdot}8\text{ mA}} = 250 \times 10^3.$$

Let it be 270 kΩ.

*Cathode resistor* $R_K$.

$$R_K = \frac{V_K}{I_A + I_S}.$$

An estimate for $V_K$ is half- way between $V_{Gc/o}$ and zero, i.e. +2 V.

$$R_K = \frac{2\text{ V}}{2{\cdot}8\text{ mA}} = 714\,\Omega.$$

Let it be the preferred value of 680 Ω.

Although the procedure given above may seem to be somewhat arbitrary, the negative feedback implicit in cathode biasing, and current operation of the screen grid, will ensure that operation will conform reasonably closely to that estimated (Fig.3.23).

If an EF91 valve is used in place of the 6AU6, the performance is comparable, although the $g_m$ of the former valve is

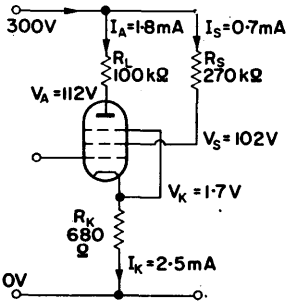



FIG 3.23. D.C. voltages for a 6AU6 (EF94).

considerably higher, giving a higher gain (250 compared with 220). The ratio of screen current to anode current (the partition factor) is smaller for the EF91 and it may be desirable to increase $R_S$ from 270 to 390 kΩ to raise $V_A$ (see Fig. 3.24).

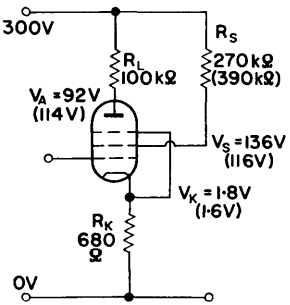



FIG. 3.24. D.C. voltages for a 6AM6 (EF91), for $R_S$ = 270 kΩ and (figures in brackets) 390 kΩ.

*Coupling network.* For the network in Fig. 3.1 the time constant associated with the coupling capacitor is

$$T_2 = C_C\left(R_G + \frac{r_a R_L}{r_a + R_L}\right) \quad \text{[from eqn. (3.6)]}$$

$$\doteqdot C_C(R_G + R_L).$$

Let the low frequency bandwidth limit be $f_2 = 50$ c/s, to ensure that the overall amplifier specification is obtained.

Therefore

$$\omega_2 = 314 \text{ r/s}$$

and

$$T_2 = 3{\cdot}19 \times 10^{-3} \text{ sec.}$$

For $R_G = 470$ kΩ,

$$C_C = \frac{T_2}{R_G + R_L} = \frac{3{\cdot}2 \times 10^{-3}}{570 \times 10^3},$$

$$= 0{\cdot}0056 \ \mu\text{F}.$$

A suitable value for $C_C$ would be 0·005 μF.

*Bypass capacitors $C_K$, $C_S$.* The bypass capacitors for both the screen and cathode can be found by trial. If with an input signal of 50 c/s, the output is observed on an oscilloscope, values of $C_K$ and $C_S$ can be found that give the maximum amplitude and any further increase in size has no effect.

Alternatively, the values can be calculated using eqns. (3.8) and (3.15).

*Cathode bypass capacitor.* So as not to affect appreciably the 50 c/s bandwidth limit, let

$$f'_K = 10 \text{ c/s}, \quad \text{i.e.} \quad \omega'_K = 62{\cdot}8 \text{ r/s}$$

$$T'_K = 15{\cdot}9 \times 10^{-3} \text{ sec}$$

$$= \frac{C_K R_K}{1 + g_m R_K} \quad \text{from eqn. (3.8) (for } R_L \ll r_a\text{).}$$

Thus,

$$C_K = \frac{T'_K(1 + g_m R_K)}{R_K} = \frac{15{\cdot}9 \times 10^{-3}(1 + 2 \times 0{\cdot}68)}{680},$$

$$= 55\ \mu\text{F}.$$

A 50 μF low voltage electrolytic capacitor would be suitable. The cathode network causes the gain to fall at 6 dB/octave below 10 c/s. This fall continues until

$$\omega_K = \frac{1}{C_K R_K} = \frac{1}{55 \times 10^{-6} \times 680} = 27\ \text{r/s},$$

i.e. $$f_K = 4{\cdot}3\ \text{c/s}.$$

Both the cathode and screen networks provide phase advance and it is, in many cases, desirable that the two maxima do not occur at the same frequency.

*Screen bypass capacitor.* Let the upper frequency

$$f'_S = 4\ \text{c/s}, \quad \text{so that} \quad \omega'_S = 25{\cdot}1\ \text{r/s}.$$

$$T'_S = 39{\cdot}8 \times 10^{-3} = \frac{r_s}{r_s + R_S} C_S R_S \quad \text{[from eqn. (3.15)]}$$

$$= \frac{A_S}{A_o} C_S R_S.$$

$A_S = -20 \quad (C_S = 0).$

$A_o = -220 \quad (R_S \text{ fully bypassed}).$

If the appropriate value of $r_s$ is not known (it frequently is not), it can be found by measuring $A_S$ and $A_o$. However, the latter values can be directly used in the above equation.

Thus,

$$C_S = \frac{T_S'}{R_S} \cdot \frac{A_o}{A_S} = \frac{1}{25{\cdot}1 \times 270 \times 10^3} \times \frac{220}{20} = 1{\cdot}62\ \mu\text{F}.$$

$$T_S = C_S R_S = 1{\cdot}62 \times 10^{-6} \times 270 \times 10^3 \text{ sec}$$

$$= 438 \times 10^{-3} \text{ sec}.$$

$$\omega_S = 2{\cdot}3 \text{ r/s} \quad \text{and} \quad f_S = 0{\cdot}37 \text{ c/s}.$$

Let

$$C_S = 2\ \mu\text{F}.$$

*High frequency response.* The h.f. time constant is $T_1 = C_S R$, where $C_S$ is the total shunt capacitance and $R$ is the total shunt resistance.

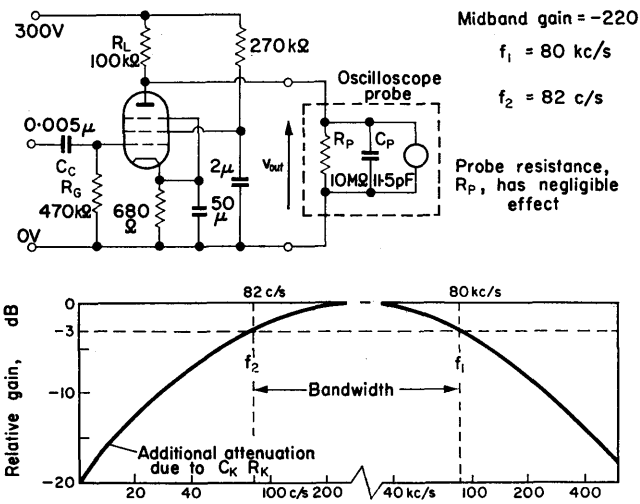



FIG. 3.25. Measured amplitude response for a 6AU6 pentode amplifier. From the value of $f_1 = 80$ kc/s, the total shunt capacitance is 22 pF, of which 12 pF is contributed by the measuring instrument. The amplifier stray capacitance is thus 10 pF.

The shunt capacitance is made up of the output capacitance of the valve, the wiring capacitance and the estimated input or load capacitance, giving a total of approximately 15 pF.

An estimate for the total shunt resistance is 80 kΩ (100 kΩ shunting the $r_a$ of the valve). Thus, $T_1 = 1{\cdot}2 \times 10^{-6}$ sec, so that $\omega_1 = 830 \times 10^3$ r/s and $f_1 = 130$ kc/s (see Fig. 3.25).

*Use of cathode follower output.* If the pentode operates into a cathode follower, the performance of the pentode amplifier is made independent of the load. In the previous example the gain

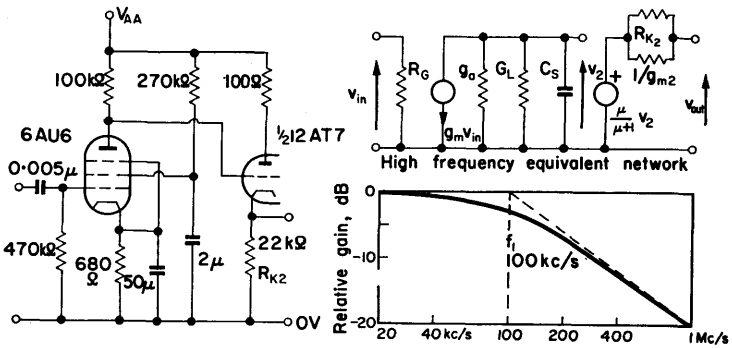



FIG. 3.26. Amplifier with cathode follower output. The bandwidth is increased to 100 kc/s, and the output stage adds 8 pF stray capacitance to the 10 pF of the pentode stage.

is a function of the external load resistance, and any added capacitance reduces the bandwidth. The cathode follower adds shunt capacitance made up principally of $C_{ga}$, the grid to anode interelectrode capacitance and socket capacitance.

Using the technique employed in Design Example 6.2, let the valve current be 5 mA.

Then,

$$R_{K2} = \frac{100\text{ V}}{5\text{ mA}} \doteqdot 22\text{ k}\Omega.$$

This is shown in Fig. 3.26.

## 3.13. High Frequency Performance of Capacitively Coupled Transistor Amplifiers

Effects similar to those associated with valve amplifiers are present, but because of the nature of transistor operation the approach to amplifier design is different.

The hybrid equivalent network of Fig. 3.27 can be modified to form a network similar to the low frequency $h$ parameter network with the feedback generator zero. This is a reasonable

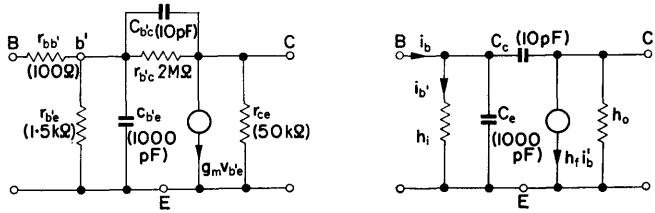



FIG. 3.27. Modified hybrid network.

approximation as the input resistance does not change greatly, for even quite large load resistance variations (see Fig. 2.26).

The resistance $r_{bb'}$, the ohmic resistance between the active base region and the base lead, is sufficiently small in this type of network to be neglected. The two capacitances which affect performance are $c_e$, the capacitance across the emitter–base junction, and $c_c$ the depletion layer capacitance across the reverse biased collector–base junction. The reverse bias clears the majority charge carriers from the junction area which acts as the dielectric of a capacitor. Capacitance $c_c$ is proportional to $1/\sqrt{V_{CB}}$. This simplified network enables rapid assessment of performance with adequate accuracy.

*Output Short Circuited* (Fig. 3.28)

The feedback capacitance $c_c$ can be neglected as it is shunted by $c_e$ which is 100 times larger. At low frequencies $i_b' = i_b$, but

at higher frequencies $h_i$ is bypassed by $c_e$ and the output current $h_f i_b'$ is reduced:

$$i_b' = \frac{1/sc_e}{h_i + (1/sc_e)} i_b = \frac{i_b}{1 + sc_e h_i}. \tag{3.25}$$

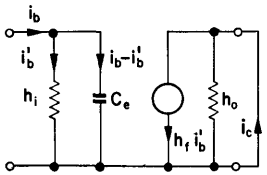



FIG. 3.28. Equivalent network with output short circuited.

$i_c/i_b = h_f/(1 + sT_B)$, where $T_B = c_e h_i$.

Short circuit current gain,

$$\frac{i_c}{i_b} = \frac{h_f}{1 + sT_B} \quad \text{(where } T_B = c_e h_i\text{)}. \tag{3.26}$$

EXAMPLE. $h_i = 2{\cdot}2\ \text{k}\Omega$ and $c_e = 700\ \text{pF}$.
Then

$$T_B = 1{\cdot}54 \times 10^{-6}\ \text{sec}$$

and

$$f_1 = \frac{10^6}{2\pi \times 1{\cdot}54}\ \text{kc/s} = 103\ \text{kc/s}.$$

Thus the relative short circuit current gain can be represented by a simple lag with a breakpoint at 103 kc/s, as shown in Fig. 3.29.

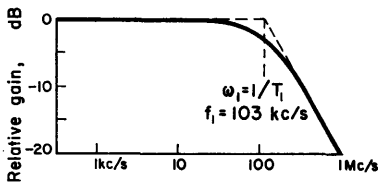



FIG. 3.29. Relative gain against frequency for short circuit output. Input is considered as a passive lag.

*Load Conductance $G_L$*

When the output is not a short circuit, as in Fig. 3.30, the effect of $c_c$ may not be negligible.

The current in $c_c$ is now

$$i_2 = (v_b - v_c)\, sc_c \quad \text{where} \quad v_c = -i_c/G_L. \tag{3.27}$$

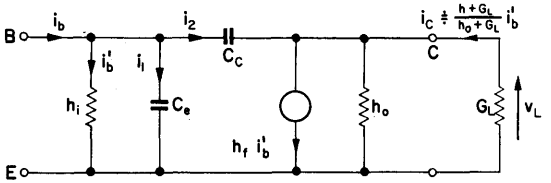



FIG. 3.30. Network including the load $G_L$.

But,

$$i'_b = \frac{v_b}{h_i}, \quad \text{and} \quad v_c = \frac{-h_f}{h_0 + G_L} \cdot \frac{v_b}{h_i},$$

or

$$v_c = -g'_m R v_b \left( \text{where } g'_m = \frac{h_f}{h_i} \quad \text{and} \quad R = \frac{1}{h_o + G_L} \right).$$

Substituting for $v_c$ in eqn. (3.27),

$$i_2 = (1 + g_m R)\, sc_c v_b = (1 - A_v)\, sc_c v_b$$

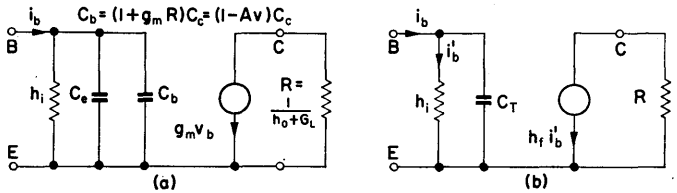



FIG. 3.31. Simplified representation of a transistor with a resistive load.

where the voltage gain $A_v = v_c/v_b$, and $c_c$ can be replaced by a capacitor $(1 + g_m R)\, c_c$ in parallel with $c_e$ as in Fig. 3.31a.

The direct effect of $c_c$ on the collector is negligible compared with the base time constant and, in most cases, the collector can be represented as in Fig. 3.31 b. Using Fig. 3.31 b the h.f. breakpoint can be determined.

*Current Gain at h.f.*

$$A_i = \frac{A_o}{1 + sT_1}, \tag{3.28}$$

where

$$A_o = \frac{G_L}{h_0 + G_L} \quad \text{and} \quad T_1 = h_i C_T.$$

EXAMPLE. $h_i = 2{\cdot}2\ \text{k}\Omega$, $c_e = 700$ pF, $c_c = 10$ pF, $R_C = 1\ \text{k}\Omega$, $h_f = 100$ and $1/h_0 = 25\ \text{k}\Omega$.

$$A_v = -\frac{h_f}{h_i(G_L + h_o)} = -\frac{100}{2{\cdot}2 \times 10^3 \times (1000 + 40)10^{-6}}$$

$$= -44.$$

$$c_b = (1 - A_v)\, c_c = 45 \times 10\ \text{pF} = 450\ \text{pF}.$$

$$C_T = c_e + c_b = 1150\ \text{pF}.$$

$$T_1 = C_T h_i = 1150 \times 10^{-12} \times 2{\cdot}2 \times 10^3$$

$$= 2{\cdot}5 \times 10^{-6}\ \text{sec}.$$

$$\omega_1 = \frac{1}{T_1} = 400 \times 10^3\ \text{r/s}.$$

$$f_1 = \frac{\omega_1}{2\pi} = 64\ \text{kc/s}.$$

The frequency response curves for a typical alloy transistor with various collector resistors are shown in Fig. 3.32.

Thus if $h_i$, $h_f$, $h_o$, $c_e$ and $c_c$ are known the high frequency response can be estimated.

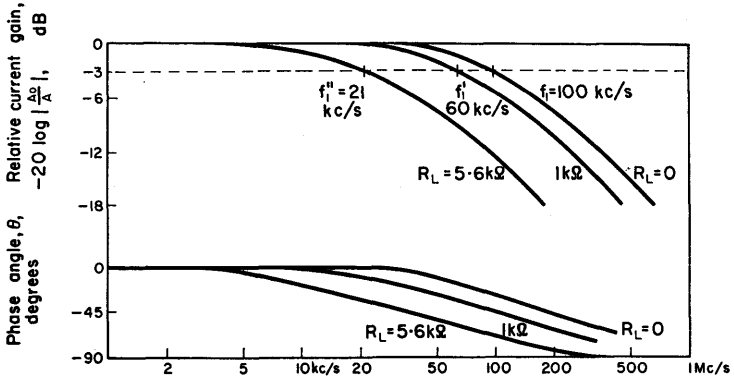



FIG. 3.32. Frequency response for an OC44 transistor with various collector resistors.

*Measurement of $c_e$ and $c_c$*

Values of $c_e$ and $c_c$ for a particular transistor can be found by finding the time constant $T_1$,

(a) with output short circuit $T_1(a)$,
(b) with known load resistance $T_1(b)$.

$T_1$ is determined by finding the frequency at which the current gain $A_0$ falls by 3 dB to 0·7 $A_0$ in each of the above cases. For case (a)

$$h_i = \frac{V_{be}}{i_b} \quad \text{and} \quad c_e = \frac{T_{1(a)}}{h_i}. \tag{3.29}$$

Time constant $T_1(b)$ is found for a load resistance $R_C$ giving a voltage gain of the order of 100 ($A_v = v_{ce}/v_{be}$).

$$C_T = \frac{T_{1(b)}}{h_i}, \tag{3.30}$$

$$c_b = C_T - c_e. \tag{3.31}$$

But,

$$C_T = (1 - A_v)\, c_c + c_e. \tag{3.32}$$

Therefore

$$c_b = (1 - A_v)\, c_c, \tag{3.33}$$

or

$$c_c = \frac{C_T - c_e}{1 - A_v}. \tag{3.34}$$

EXAMPLE.

$A_v = \dfrac{v_{ce}}{v_{be}} = -209$ (negative sign indicates signal inversion).

$$h_i = \frac{v_{be}}{i_b} = \frac{22\text{ mV}}{10\ \mu\text{A}} = 2{\cdot}2\ \text{k}\Omega.$$

For $R_C = 100\,\Omega$ (output effectively short circuited), $f_1 = 100$ kc/s,

$$\omega_1 = 628 \times 10^3\ \text{r/s},$$

and

$$T_1 = 1{\cdot}6 \times 10^{-6}\ \text{sec}.$$

Therefore

$$c_e = \frac{1{\cdot}6 \times 10^{-6}}{2{\cdot}2 \times 10^3} = 730\ \text{pF} \quad \text{[using eqn. (3.29)]}.$$

For $R_C = 5{\cdot}6$ kΩ, $f_1 = 21$ kc/s, $\omega_1 = 132 \times 10^3$, and $T_1 = 7{\cdot}6 \times 10^{-6}$ sec.

Therefore

$$C_T = \frac{7{\cdot}6 \times 10^{-6}}{2{\cdot}2 \times 10^{-3}} = 3460\ \text{pF} \quad \text{[using eqn. (3.30)]},$$

$$c_b = C_T - c_e = 2730\ \text{pF} \quad \text{[eqn. (3.31)]},$$

$$c_c = \frac{c_b}{1 - A_v} = \frac{2730}{210} = 13\ \text{pF} \quad \text{[from eqn. (3.33)]}.$$

## 3.14. LOW FREQUENCY PERFORMANCE OF CAPACITIVELY COUPLED STAGES

As the frequency is reduced the increased impedance of $C_C$ reduces $i_{in}$, the transistor input current (see Fig. 3.33).

At frequencies where $r_{in}$ is much greater than $1/\omega C_C$,

$$i_{in} = \frac{R_{out}}{R_{out} + r_{in}} \cdot i \quad (\text{if} \quad R_B \gg r_{in}),$$

and for efficient current transfer, $r_{in}$ should be much less than $R_{out}$.

If $i$ is the current from the transistor of the previous stage, $R_{out}$ will be the resistance of $1/h_0$ in parallel with $R_C$ for that

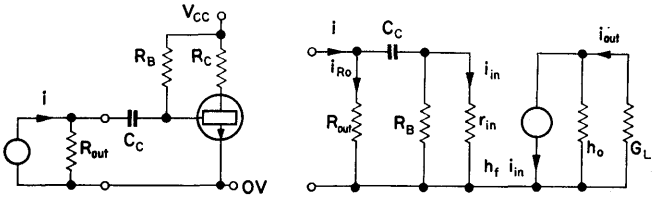



FIG. 3.33. Capacitively coupled amplifier with low frequency equivalent network.

stage. If these two terms are both 20 kΩ, $R_{out}$ will be 10 kΩ and for $r_{in}$ of 2 kΩ the current transfer $i_{in}/i = 10\ \text{k}\Omega/(10\ \text{k}\Omega + 2\ \text{k}\Omega) = 5/6$.

For efficient transfer, $R_C$ should be as large as possible.

At low frequencies

$$i_{in}(s) = \frac{R_{out}}{R_{out} + r_{in} + (1/sC_C)} \cdot i(s). \tag{3.35}$$

The current transfer falls by 3 dB when $R_{out} + r_{in} = 1/\omega C_C$ or

$$\omega = \frac{1}{C_C(R_{out} + r_{in})} = \frac{1}{T_2}, \tag{3.36}$$

where $T_2 = C_C(R_{out} + r_{in})$.

Equation (3.36) can be rewritten with the frequency invariant components extracted:

$$i_{in}(s) = \frac{R_{out}}{R_{out} + r_{in}} \cdot \frac{1}{1 + (1/sT_2)}\, i(s), \tag{3.37}$$

$$i_{out}(s) = A_0 i_{in} \quad \left(\text{where} \quad A_0 = \frac{h_f G_L}{h_0 + G_L}\right)$$

$$= A_0 \frac{R_{out}}{R_{out} + r_{in}} \cdot \frac{1}{1 + (1/sT_2)}\, i(s)$$

$$= A_2 \frac{1}{1 + (1/sT_2)}\, i(s) \tag{3.38}$$

$$\left(\text{where} \quad A_2 = A_0 \cdot \frac{R_{out}}{R_{out} + r_{in}}\right).$$

For coupling capacitor $C_C$,

$$A(s) = A_2 \frac{1}{1 + (1/sT_2)}. \tag{3.39}$$

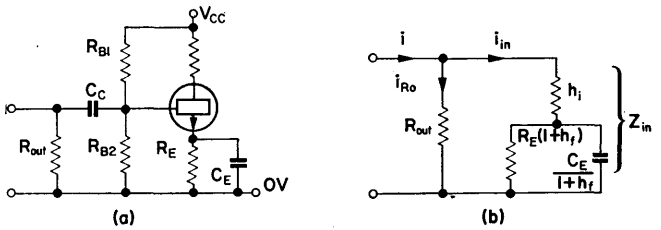



FIG. 3.34. Input network neglecting bias resistors and coupling capacitor. $R_O$ includes $R_B$.

*Effect of Emitter Capacitor on Low Frequency Performance*

If an emitter resistor $R_E$ is used for stabilization (see § 2.11), usually a bypass capacitor $C_E$ will be employed to increase gain at signal frequencies.

At sufficiently low frequency (or if $C_E$ is not present), the input resistance of the transistor is increased from $h_i$ to $h_i+(1+h_f)R_E$. This follows from considerations given in § 2.12, and shown in Fig. 3.34.

$$z_{in}(s) = h_i + (1 + h_f)\, Z_E,$$

$$= h_i + (1 + h_f)\frac{R_E}{1 + sC_ER_E}.$$

This should be inserted in place of $r_{in}$ for the expression for $A_2$ in eqn. (3.38).

Thus,

$$A_2(s) = \frac{R_{out}}{R_{out} + z_{in}} A_0$$

$$= \frac{R_{out}}{R_{out} + h_i + (1 + h_f)\,[R_E/(1 + sC_ER_E)]} A_0$$

$$= \frac{R_{out}}{R_{out} + h_i + (1 + h_f)\, R_E} \times$$

$$\times \frac{1 + sC_ER_E}{1 + \{sC_ER_E(R_{out} + h_i)/[R_{out} + h_i + (1 + h_f)\, R_E]\}} A_0. \tag{3.40}$$

Thus, gain expression for partially bypassed emitter resistor is

$$A(s) = A_E \frac{1 + sT_E}{1 + sT'_E},$$

where

$$A_E = \frac{R_{out}}{R_{out} + h_i + (1 + h_f)\, R_E} A_0, \tag{3.41}$$

$$T_E = C_ER_E \quad \text{and} \quad T'_E = \frac{T_E(R_{out} + h_i)}{R_{out} + h_i + (1 + h_f)\, R_E}.$$

$$T_E > T'_E.$$

This is illustrated in Fig. 3.35.

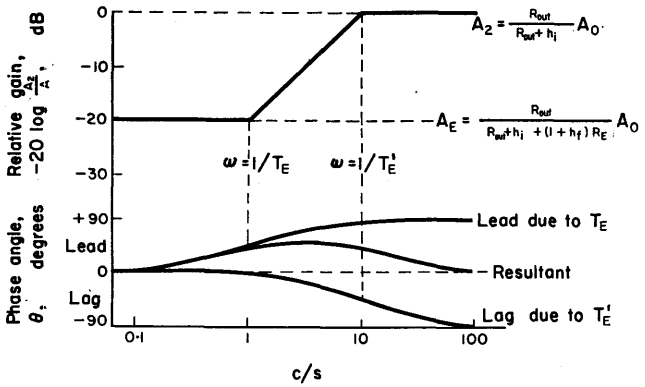



FIG. 3.35. Effect of emitter time constant on amplifier performance.
$C_E R_E = 1$ c/s and $A_2/A_E = 10$.

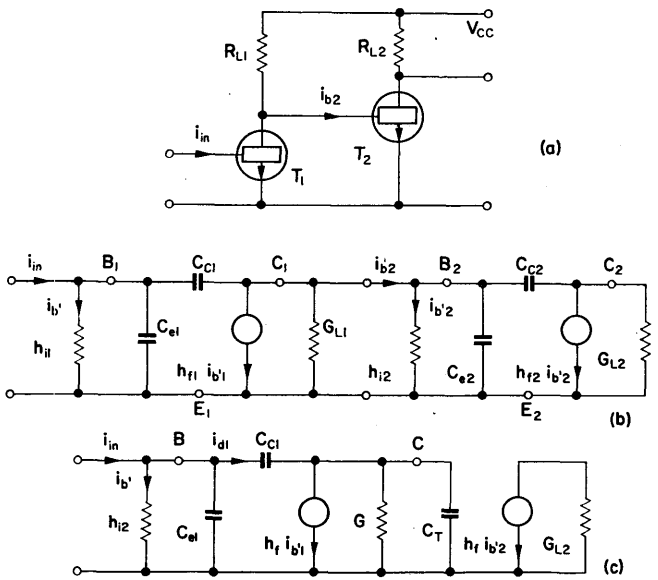



FIG. 3.36. Reduction of the equivalent network of a two-stage amplifier to estimate h.f. performance.

## 3.15. Tandem Stages of Transistor Amplifier

If one transistor is followed by another, the first has the input impedance of the second as its load impedance.

In Fig. 3.36b the effect of the collector capacitance $c_{c2}$ is to augment $c_{e2}$ giving rise to $C_T$ of Fig. 3.36c.

Part of the input current will flow in $c_{c1}$, the amount being determined by the voltage gain between the base and collector. The voltage gain of $T_1$ is complex, because the collector load is $G$ and $C_T$ in parallel.

The voltage gain between $B$ and $C$,

$$A_{v1} = -\frac{g_m R}{1 + sT}, \tag{3.42}$$

where $T = C_T/G$ and $R = 1/G$.

Thus,

$$i_{d1} = v_{be}\left(1 + \frac{g_m R}{1 + sT}\right) sc_{c1},$$

and the impedance to be shunted across the base of $T_1$ by $c_{c1}$ is

$$Z(s) = \frac{1 + sT}{[(1 + g_m R) + sT]\, sc_{c1}},$$

or

$$Z(j\omega) = \frac{1 + j\omega T}{j\omega c_{c1}(1 + g_m R + j\omega T)}. \tag{3.43}$$

Separating real and imaginary components,

$$Z(j\omega) = \frac{1 + g_m R + (\omega T)^2}{j\omega c_{c1}(1 + g_m R)^2 + (\omega T)^2} + \frac{T g_m R}{c_{c1}[(1 + g_m R)^2 + (\omega T)^2]} \tag{3.44}$$

$$\doteqdot \frac{1}{j\omega c_{c1} \cdot g_m R} + \frac{C_T}{c_{c1} g_m} \quad \text{as} \quad g_m R \gg 1, \tag{3.45}$$

and for frequencies where $\omega T < 1$.

The added impedance is a resistance $C_T/c_{c1}g_m$ in series with capacitance $c_{c1}g_mR$. The resulting simplified network is shown in Fig. 3.37.

DESIGN EXAMPLE 3.3

Required, an amplifier stage with transfer resistance of 100 kΩ and bandwidth from 50 c/s to 20 kc/s. The signal source resistance is 5 kΩ and a peak output of 4 V is required. (Transfer resistance $= v_{out}/v_{in}$.)

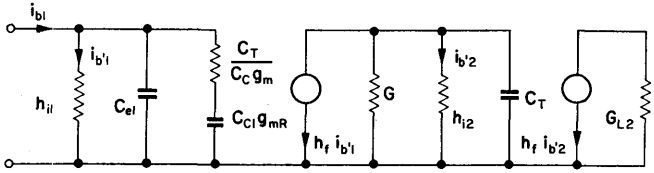



FIG. 3.37. Equivalent network of a two stage transistor amplifier with collector-to-base coupling eliminated. Note that a resistance and capacitance in series appears across the input.

Using emitter stabilization a starting point is $R_B/R_E = 5$ (§ 2.11) where

$$R_B = \frac{R_{B1}R_{B2}}{R_{B1} + R_{B2}}.$$

For a nominal $h_f = 50$ (minimum value for OC44),

$$K = 1 + \frac{h_f R_E}{R_E + R_B} = 1 + \frac{50 \times 1}{1 + 5} = 9{\cdot}3.$$

*Supply voltage.* To obtain an output voltage swing of 8 V peak to peak, $V_{CC} = -12$ V is suitable.

*Collector resistor.*

$$R_T = \frac{h_f}{G_C + h_o} \doteq \frac{h_f}{G_C} \quad (\text{for } h_o \ll G_C).$$

The transfer resistance of 100 kΩ requires a collector resistor of 2·2 kΩ. Let the value 2·7 kΩ be used to allow for the reduction in current gain by the bias network.

*Collector current.* For the required output voltage $V_C = -7{\cdot}5\,\text{V}$.

$$I_C = \frac{V_{CC} - V_C}{R_C} = \frac{4{\cdot}5\,\text{V}}{2{\cdot}7\,\text{k}\Omega} = 1{\cdot}7\,\text{mA}.$$

*Emitter resistor.* Allowing 2·5 V across the emitter resistor, and as $I_E = I_C$,

$$R_E \doteqdot \frac{V_E}{I_E} = \frac{2{\cdot}5\,\text{V}}{1{\cdot}7\,\text{mA}} = 1{\cdot}5\,\text{k}\Omega.$$

*Base resistors* $R_{B1}$, $R_{B2}$. $R_B$, which is $R_{B1}$ and $R_{B2}$ in parallel $= 5\,R_E = 7{\cdot}5\,\text{k}\Omega$.

$$V_B = V_{BE} + V_E$$

$$= -0{\cdot}15\,\text{V} - 2{\cdot}5\,\text{V} \quad \text{for a germanium transistor}$$

$$= -2{\cdot}65\,\text{V}.$$

Neglecting the base current $I_B$,

$$\frac{V_B}{V_{CC}} = \frac{2{\cdot}65\,\text{V}}{12\,\text{V}} = 0{\cdot}22$$

$$= \frac{R_{B1}}{R_{B1} + R_{B2}} = \frac{R_B}{R_{B2}} = \frac{5\,R_E}{R_{B2}}.$$

Thus,

$$R_{B2} = \frac{5\,R_E}{0{\cdot}22} = \frac{5}{0{\cdot}22} \times 1{\cdot}5\,\text{k}\Omega = 34\,\text{k}\Omega.$$

Also,

$$\frac{R_{B1}}{R_{B2}} = \frac{2{\cdot}65\,\text{V}}{9{\cdot}35\,\text{V}},$$

therefore

$$R_{B1} = \frac{2{\cdot}65}{9{\cdot}35} \times 34\,\text{k}\Omega = 9{\cdot}65\,\text{k}\Omega.$$

Let $R_{B1} = 9{\cdot}1\,\text{k}\Omega$ and $R_{B2} = 33\,\text{k}\Omega$. The d.c. conditions are shown in Fig. 3.38.

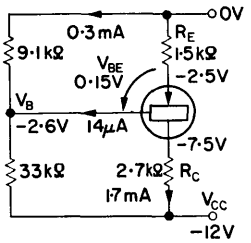



FIG. 3.38. D.C. conditions for a transistor amplifier stage.

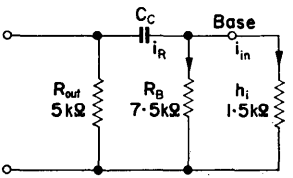



FIG. 3.39. Equivalent network to show the effect of $R_B$ shunting $h_i$, assuming $R_E$ to be fully bypassed by $C_E$.

$R_B$ shunts the input of the transistor and reduces the gain, as in Fig. 3.39.

The input resistance $h_i$ to the transistor is nominally 1·5 kΩ for a collector current of 1·7 mA.

$$R'_T = \frac{R_E}{R_B + h_i} \cdot \frac{h_f}{G_C + h_o}$$

$$= \frac{7{\cdot}5\,\text{k}\Omega}{7{\cdot}5\,\text{k}\Omega + 1{\cdot}5\,\text{k}\Omega} \times$$

$$\times \frac{50}{370 \times 10^{-6} + 50 \times 10^{-6}} \doteqdot 100\,\text{k}\Omega.$$

*Coupling capacitor.*

$$T_2 = C_C(R_{out} + r_{in}) = \frac{1}{\omega_2}, \quad \text{from eqn. (3.36),}$$

where $r_{in}$ is resistance of $R_B$ and $h_i$ in parallel (= 1·1 kΩ).
It is required that $f_2 = 50$ c/s, or $\omega_2 = 214$ r/s.
Therefore

$$T_2 = 3{\cdot}19 \times 10^{-3} \text{ sec.}$$

$$C_C = \frac{T_2}{R_{out} + r_{in}} = \frac{3{\cdot}19 \times 10^{-3}}{5\ \text{k}\Omega + 1{\cdot}1\ \text{k}\Omega} = 0{\cdot}523\ \mu\text{F.}$$

Let $C_C$ be a 1 μF electrolytic capacitor.

*Emitter resistor bypass capacitor.*

$$T_E' = \frac{T_E(R_{out}' + h_i)}{R_{out}' + h_i + (1 + h_f)\,R_E}, \quad \text{from eqn. (3.41),}$$

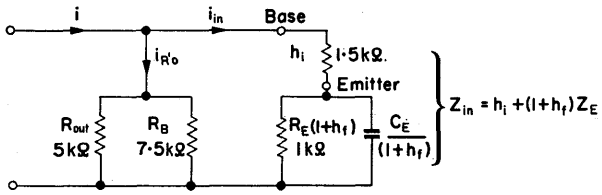



FIG. 3.40. Division of input current between $R_{out}'$ and base.

where $R_{out}'$ is $R_{out}$ in parallel with $R_B$, as in Fig. 3.40.

$$\frac{T_E'}{T_E} = \frac{R_{out}' + h_i}{R_{out}' + h_i + (1 + h_f)\,R_E}$$

$$= \frac{3\ \text{k}\Omega + 1{\cdot}5\ \text{k}\Omega}{3\ \text{k}\Omega + 1{\cdot}5\ \text{k}\Omega + (1 + 50)\,1{\cdot}5\ \text{k}\Omega}$$

$$\doteqdot 0{\cdot}06.$$

To ensure that the emitter impedance does not affect the gain at 50 c/s let $T_E'$ be $5T_2 = 1{\cdot}6 \times 10^{-2}$. The breakpoint $T_E'$ will be at 62·8 r/s, i.e. 10 c/s.

$$T_E' = T_E \times 0{\cdot}06,$$

therefore

$$C_E = \frac{T_E}{R_E} = \frac{1{\cdot}6 \times 10^{-2}}{0{\cdot}06 \times 1{\cdot}5 \times 10^3} = 175\ \mu\text{F}.$$

Let $C_E$ be 200 μF.

*High frequency performance.* This is a function of the transistor capacitances $c_e$ and $c_c$.

From Fig. 3.32 it is apparent that, with $R_C = 2{\cdot}7\ \text{k}\Omega$, a 20 kc/s upper frequency limit can be obtained. The completed design is shown in Fig. 3.41.

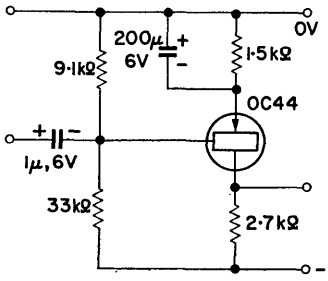



FIG. 3.41. Capacitively coupled transistor amplifier stage of Design Example 3.3.

DESIGN EXAMPLE 3.4

Required, an amplifier with voltage gain greater than −50,000 over a frequency range of 100 c/s to 10 kc/s. The required peak output voltage is 10 V.

*Voltage gain.* $A_V = R_L A_i / r_{in}$, where $A_i$ is the over-all current gain, $R_L$ is the effective load resistance, and $r_{in}$ is the input resistance to the amplifier.

To provide the necessary current gain and signal inversion, three stages are required.

Let the transistors be 2S 103 which are silicon mesa types with voltage rating $V_{CEO} = 40$ V and $h_{fe(\min)} = 50$. As shown in Fig. 3.42, these can be directly coupled (see § 6.5). Estimating the

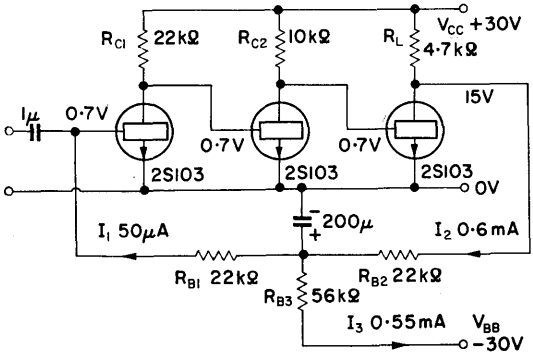



FIG. 3.42. Direct coupled three-stage transistor amplifier with zero frequency stabilization. Since the current through $R_{B1}$ and the voltage at the input base are both small, the junction of $R_{B1}$, $R_{B2}$ and $R_{B3}$ must be at approximately 0 V. Thus the ratio of the voltages across $R_{B2}$ and $R_{B3}$ is directly proportional to their resistance, i.e. $V_C = R_{B2}/R_{B3} \cdot V_{BB}$.

minimum effective current gain of each stage as 30, the overall current gain $A_i = 27{,}000$.

*Load resistor* $R_L$. If the input transistor is run at a current that gives $r_{in} = 2\,\text{k}\Omega$,

$$R_L = \frac{A_v}{A_i} r_{in} \doteq \frac{50{,}000}{27{,}000} \times 2\,\text{k}\Omega = 3{\cdot}7\,\text{k}\Omega.$$

To allow for loading by the bias network and $h_o$, let $R_L = 4{\cdot}7\,\text{k}\Omega$.

*Collector supply voltage* $V_{CC}$. As the peak to peak output voltage is 20 V let $V_{CC} = 30$ V.

*Collector resistors*, $R_{C1}$ and $R_{C2}$. For $T_1$ to be run at 1·5 mA, $R_{C1} = 20\,\text{k}\Omega$ and for $T_2$ to be run at 3·0 mA, $R_{C2} = 10\,\text{k}\Omega$.

*Bias network.* At operating frequency, $R_{B1}$ and $R_{B2}$ shunt the input and output respectively. To minimize shunting effects let them both be 22 kΩ, as in Fig. 3.42.

The estimated input current

$$I_1 = \frac{I_{C1}}{h_{fe}} \doteqdot \frac{1{\cdot}5\,\text{mA}}{30} = 50\,\mu\text{A}.$$

This current, flowing in $R_{B1}$, will produce 1·1 V, which must be added to $V_{BE} = 0{\cdot}7$ V to give the voltage at the junction of $R_{B1}$ and $R_{B2}$. This is approximately 2 V.

For a collector voltage for $T_3$ of 15 V, the current in $R_{B2}$,

$$I_2 = \frac{15\,\text{V} - 2\,\text{V}}{22\,\text{k}\Omega} \doteqdot 0{\cdot}6\,\text{mA}.$$

$R_{B3}$ must take the difference in current between $I_2$ and $I_1$, that is

$$I_3 \doteqdot 0{\cdot}55\,\text{mA}.$$

For

$$V_{BB} = -30\,\text{V}, \quad R_{B3} = \frac{30\,\text{V} + 2\,\text{V}}{0{\cdot}55\,\text{mA}} = 58\,\text{k}\Omega.$$

Let the value be 56 kΩ.

*Bypass capacitor* $C_B$. The d.c. stabilization is due to negative feedback provided by the bias network. To eliminate feedback at signal frequency, the capacitor $C_B$ is used. A value of 200 μF reduces the feedback by a factor of 3000 at 100 c/s.

*Input capacitor.* From eqn. (3.36),

$$\omega = \frac{1}{C_C(R_{\text{out}} + r_{\text{in}})},$$

or

$$C_C = \frac{1}{\omega r_{in}} \quad \text{if } R_{out}\text{, the source resistance, is zero.}$$

(This gives the maximum value of $C_C$.)

For

$$\omega = 628 \text{ r/s} \quad (f = 100 \text{ c/s}),$$

$$C_C = \frac{1}{628 \times 2 \text{ k}\Omega} = 0{\cdot}8 \ \mu\text{F}.$$

Let

$$C_C = 1 \ \mu\text{F}.$$

The completed circuit is shown in Fig. 3.42.

CHAPTER 4

# Power Amplifiers

## 4.1. The Class A Power Amplifier

In a power amplifier the object is to obtain the maximum amount of power from a given valve, while limiting the distortion to a predetermined level. Under Class A conditions the operation is confined to that part of the dynamic characteristic which is reasonably linear, and anode current flows during the whole period of signal input. Assuming the dynamic characteristic to be a straight line, the anode efficiency may be written as:

$$\text{Anode efficiency} = \frac{\text{Power in load}}{V_0 I_0}$$

$$= 0{\cdot}5\left(1 - \frac{V_{\min}}{V_0}\right)\left(1 - \frac{I_{\min}}{I_0}\right) \qquad (4.1)$$

(see Fig. 1.5). The maximum efficiency theoretically obtained is therefore 50%. To achieve this, however, it would be necessary for both the anode current and the anode voltage to swing to zero and in practice, due to curvature of the characteristic, this would give rise to an undesirable level of distortion. When operated in such a manner as to keep distortion to a minimum, efficiencies of 20–40% may be obtained using pentodes, while a triode would provide a somewhat lower efficiency.

### *Choice of a Valve*

Taking account of these efficiencies, a valve should be chosen having a rating considerably higher than the desired amount of

a.c. power. In general a pentode should have a rating of 3 times the required a.c. power, while if a triode is chosen, a rating of 5 times the a.c. power will be necessary. There remains the choice between a triode, a beam tetrode and a pentode. The pentode has a greater anode efficiency than the triode, particularly when operated at relatively low anode supply voltages. The beam tetrode is similarly superior in this respect. Furthermore, the triode requires a larger exciting voltage for a given power output than do the other two types of valves. However pentode and beam tetrode valves in general have much higher distortion levels in their dynamic characteristics than do triodes. Moreover this distortion contains a significant percentage of third harmonic, being greater for the pentode than for the tetrode, whereas for the triode the second harmonic is predominant.

Where the power valve is to form the output stage of an audio amplifier, this consideration used to be of the utmost importance, since it was recognized that third harmonic distortion was much more objectionable to the ear than was second harmonic distortion. With the advent of negative feedback, however, this serious limitation of the pentode or beam tetrode power amplifier ceased to be important.

*Design Considerations*

As in the voltage amplifier, the aim is to get the maximum control of anode current by allowing the grid voltage to swing as far as possible on the straight part of the characteristic. In the anode circuit, however, the power amplifier differs widely from the voltage amplifier. When a generator is feeding a resistive circuit, maximum power is transferred when the load resistance is equal to the internal resistance of the generator. In the case of a valve, conditions are somewhat different because of the need to keep distortion to a minimum. In practice the load of a triode power valve should be at least twice its $r_a$, while the load of a pentode will be less than its $r_a$.

*Design Steps*

1. Select a suitable valve, from consideration of the power requirement and acceptable distortion level.
2. Determine the operating point and construct a load line through it.
3. Calculate the grid voltage swing to provide the required power output, and determine the amount of distortion present.
4. Evaluate the cathode resistor which will provide the correct operating bias.
5. From consideration of the minimum frequency to be handled, select a suitable decoupling capacitor for the cathode resistor.

DESIGN EXAMPLE 4.1

Required, an a.c. power of 0·75 W into a resistive load, with distortion not more than 5%. An h.t. supply of 300 V is available.

*Valve.* Because of the low distortion requirement a triode is obviously necessary, or a suitable pentode may be chosen and connected as a triode. It will moreover be necessary to select a valve having a much higher rating than the specified power. Such a valve is the EL86 having an anode rating of 13 W when operated as a triode, and whose characteristics are given in Fig. 4.1.

*Load.* From the valve data sheets, the $r_a$ of the valve is given as 665 Ω, so a load may be considered of 3 times this figure, say 2·2 kΩ. If a load line for this resistance is drawn from the point $V_A = 300$, $I_A = 0$, the distortion and power output may then be calculated.

The percentage harmonic distortion is given by the expression

$$\frac{(I_{max} + I_{min} - 2I_0) \times 100}{2(I_{max} - I_{min})}. \qquad (4.2)$$

However, a quick assessment of distortion may be made by measuring the load line and calculating the ratio of its two parts.

For instance, in Fig. 4.1, with the operating point at *O*, if the ratio of *OA* to *OB* is 11 to 9, i.e. a ratio of 1·22, then 5% second harmonic distortion is present. If this figure is less than 1·22, the distortion is less than 5%, there being no distortion when the two parts are equal.

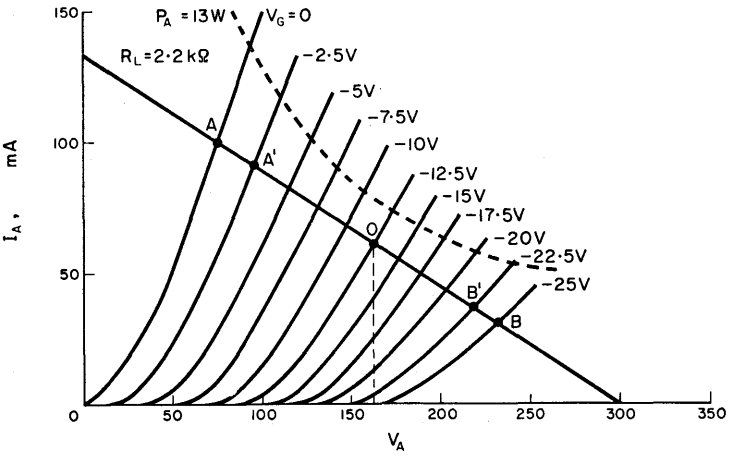



FIG. 4.1. Characteristic curves of an EL86 (triode connected), with a load line of 2·2 kΩ. Note that approximately the same amount of power is dissipated in the load as in the valve.

The power developed in the load is given by the expression

$$\text{Power} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}. \qquad (4.3)$$

For the load *AOB*, $V_{min} = 75$ V, $V_{max} = 235$ V, $I_{max} = 100$ mA and $I_{min} = 30$ mA. The a.c. power developed with an input signal of 12·5 V peak is therefore approximately 1·4 W. This is in excess of the required power output, but on measuring the ratio of *AO* to *BO* a figure of 1·3 is obtained, indicating a second harmonic content greater than 5%.

Now let the input signal be reduced to 10 V peak, as indicated by the shortened load line *A'OB'*. The power, calculated as

above, is seen to be 0·86 W and the second harmonic distortion is 5%. A 2·2 kΩ load is therefore satisfactory providing the input signal does not exceed this value. It is perfectly reasonable to limit the input voltage in this way, since in designing a complete amplifier, the output stage should be designed first, to provide the required power, then in the knowledge of the necessary signal drive, the preceding stage is arranged to supply it.

*Cathode resistor.* This must have a value such that, when carrying the standing anode current of 60 mA, it will provide a bias of 12·5 V. The correct value is therefore 210 Ω; let it be 220 Ω which is a preferred value.

*Decoupling capacitor.* At the minimum frequency at which the stage is to be used, the reactance of the decoupling capacitor should be small compared with 220 Ω. For instance, if the minimum frequency is 50 c/s, then at this frequency a 100 μF capacitor has a reactance of about one-seventh of the cathode resistor which is probably satisfactory.

The final design is therefore summed up as:

Operating point $V_A = 160$ V, $V_G = -12{\cdot}5$ V.
Anode load resistor, 2·2 kΩ.
Cathode resistor 220 Ω decoupled by 100 μF.

For operation as a triode, the screen grid is connected to the anode.

## 4.2. Audio Power Amplifier, Class A

### *Design Considerations*

The load impedance is usually coupled to the valve of a Class A power amplifier by means of a transformer, as in the case of an audio amplifier where the load is the loudspeaker. The necessity of passing the d.c. anode current through the load is thus avoided and, by a suitable choice of transformer turns ratio, the correct load impedance is offered to the valve. This enables the speech

coil of a loudspeaker to be made up of fine wire and with low impedance. Alternatively, without transformer coupling, it would be necessary to wind the speech coil with wire sufficiently thick to be able to carry the d.c. anode current, and yet having the high impedance which is necessary for the optimum transference of power from the valve. This would obviously increase the bulk of the speech coil and likewise its inertia.

With regard to distortion, the amount which may be tolerated depends largely on the type of equipment for which the stage is to be designed. To obtain a very low distortion level a poor efficiency must generally be tolerated and this would obviously be uneconomic in a domestic radio receiver for instance. For this type of equipment, listening tests have shown that a level of 5% third harmonic distortion produced on peak values of signal is not excessive. Since most pentodes and tetrodes have a second harmonic content at least equal to the third over most of the power range, it would seem that 10% total harmonic distortion would be acceptable for such equipment.

*Design Steps*

1. Select a suitable valve, choose an operating point at $V_A$ = h.t. and construct a number of load lines through it.
2. Select the load which provides the required power with an acceptable distortion level.
3. Calculate the turns ratio of the transformer to match the loudspeaker impedance to this load.
4. Determine the values of the cathode resistor and capacitor.

DESIGN EXAMPLE 4.2

Required, an a.c. power output of 4 W with third harmonic distortion not exceeding 5%. An h.t. supply of 250 V is available.

As the distortion requirement is not as exacting as in the previous example, a better anode efficiency is possible. Let the valve chosen be a 6BW6 beam tetrode with an anode rating of 13·2 W and whose characteristics are given in Fig. 4.2.

*Operating point.* Under no signal conditions the secondary of the output transformer has no effect, and only the primary need be considered. In the absence of a signal the primary inductance may be neglected, and as the primary resistance will be very low, this too may be neglected at this stage. There will therefore be no volts drop and the anode will be at the full h.t. of 250 V. The grid bias is selected to provide maximum anode current

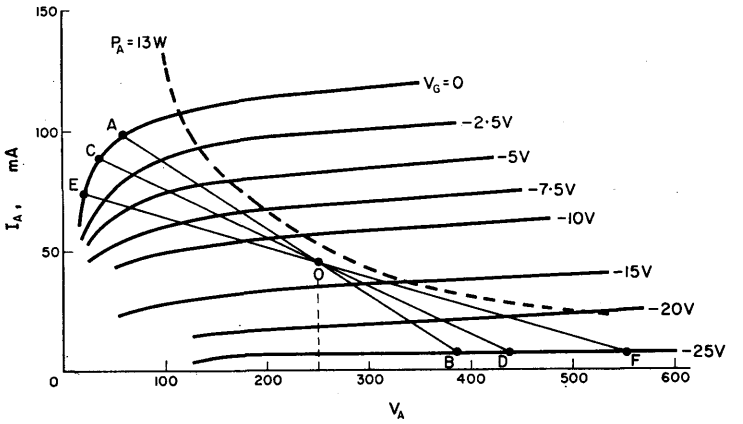



FIG. 4.2. Characteristic curves for a 6BW6 beam tetrode. The load lines drawn are for a transformer coupled load. Note that in this case the operating point is at full h.t. whereas in Fig. 4.1 it was at approximately half the h.t. voltage.

with this anode voltage, but without exceeding the valve rating. A grid voltage of $-12{\cdot}5$ V is suitable, providing for a grid swing of 25 V peak to peak. The operating point is drawn at *O* and three load lines constructed, *AOB*, *COD* and *EOF*.

*Power output.* Consider load *AOB* for an input signal swing from 0 to $-25$ V. Substituting values in eqn. (4.3),

$$\text{Power} = \frac{(385 - 60)(98 - 8) \times 10^{-3}}{8} = 3{\cdot}6 \text{ W}.$$

Similar calculations for the other two loads give power outputs

of 4·1 W for *CD* and 4·4 W for *EF*. The load represented by *AB* is rejected because its power output is insufficient. A comparison of the ratios of the two parts of each of the other load lines shows load *CD* to have less distortion than *EF*. Hence if the third harmonic distortion of the load *CD*, which is 5 kΩ, is less than 5% then this load will be suitable. There are a number of graphical methods of determining third harmonic distortion.[17] However, most manufacturers include in their data sheets a

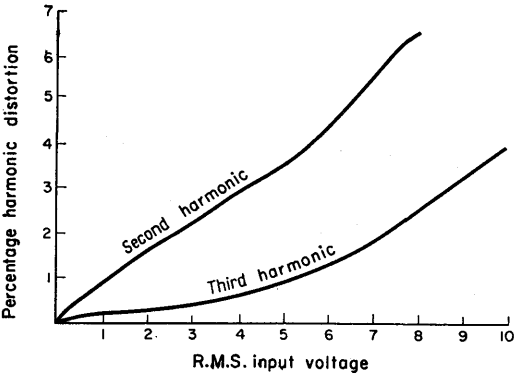



FIG. 4.3. Percentage harmonic distortion as a function of input voltage for a 6BW6 beam tetrode with a 5 kΩ load.

curve which indicates the amount of distortion present for various input voltages. Such a graph, representative of the 6BW6 with a 5 kΩ anode load is given in Fig. 4.3. A peak input voltage of 12·5 V, i.e. an r.m.s. voltage of 8·75 V, is seen to result in a third harmonic content of less than 5% so that a 5 kΩ load is acceptable. If, however, it had been greater than 5%, it would still have been possible to meet the specification by a slight reduction of input voltage.

*Transformer turns ratio.* If the nominal impedance of the speech coil is 3Ω, the turns ratio to match this to 5 kΩ is

$$n = \sqrt{\left(\frac{5000}{3}\right)} \doteqdot 41.$$

The output transformer therefore needs a step-down turns ratio of 41 to 1. Two points should here be noted. Firstly, the impedance of a loudspeaker is highly complex and varies with frequency. The impedance quoted by the makers is usually given for 1 kc/s and is largely resistive. This then is the only frequency at which correct matching is obtained. At higher frequencies the loudspeaker load becomes reactive and impedance rises. The effect of this can be largely compensated by the addition of a suitable series *R–C* circuit across the transformer primary. At the lower frequencies the impedance again rises as the electromechanical resonant frequency of the speaker is approached. Generally, negative feedback from the speech coil is used to reduce this effect.

The second fact to be noted is that the anode voltage is seen to swing to a value in excess of the available h.t. supply voltage. This is explained by the fact that the transformer inductance can produce a voltage which momentarily augments the h.t. supply, allowing the anode to swing to its peak voltage on negative swings of input signal.

*Screen resistor.* The main consideration is to ensure that the screen voltage is such that the dissipation at this electrode does not exceed the maximum specified by the makers. From the valve data sheet this maximum is given as 2·2 W. It is also noted that with a screen voltage of 250 V the current drawn is 4·5 mA, i.e. a little over 1 W. It is therefore safe to connect the screen grid to h.t. as is commonly done in this type of circuit.

*Cathode resistor.* This must have such a value that, when carrying the sum of anode and screen currents, it will have dropped across it a voltage equal to the required bias of 12·5 V. The total current is 50 mA so that the required resistance is 250 Ω. The power dissipated in this is:

$$I^2R = 2500 \times 10^{-6} \times 250 = 0{\cdot}625 \text{ W}.$$

A 250 Ω 1 W resistor will therefore be used. It must be bypassed by a capacitor having a reactance which is low compared with

250 Ω, at the lowest frequency to be handled. At 50 c/s a 100 μF capacitor has a reactance of 32 Ω which is satisfactory. The completed circuit is given in Fig. 4.4.

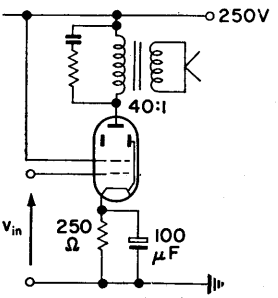



FIG. 4.4. Completed circuit of Design Example 4.2. The series *R–C* circuit can be used to compensate for changes in impedance of the loudspeaker as the frequency varies.

## 4.3. THE CLASS B PUSH–PULL AMPLIFIER

In a push–pull amplifier the two valves are excited by equal grid voltages, 180° out of phase, and the outputs are combined by means of a centre tapped transformer. The two valves, when arranged in this manner, are equivalent to a single valve having twice the $r_a$ and twice the $\mu$ of an individual valve. Assuming identical valves, the push–pull arrangement has the following advantages over a single valve stage:

(1) There is no possibility of direct current saturation in the core of the output transformer.
(2) No signal frequency currents flow in the h.t. supply source and hence there is no feedback to previous stages using the same supply.
(3) Even order harmonics cancel out, thus providing less distortion for a given amount of power.
(4) Hum voltages in the h.t. source do not give rise to hum in the output because these too cancel out.

*Choice of Valves*

In choosing valves for use in a push–pull stage, the same general considerations apply as did for the single valve power amplifier. However, in this case a pair of valves should be used which have been carefully matched. Failure to do this will increase harmonic distortion considerably. For instance, a difference of 10% in the anode currents of the two valves, measured under identical operating conditions, will give rise to approximately 5% second harmonic distortion. Valve manufacturers supply matched pairs on demand but it is necessary to state the conditions under which the valves are to be operated. It is also most important that, in use, the valve ratings should not be exceeded as this may permanently change the characteristics thus upsetting the matching.

*Design Considerations*

Under Class B conditions the grid bias is approximately equal to the cut-off value, and no current flows in the absence of an input signal. When a signal is applied to the stage, each valve conducts on alternate half-cycles. This class of amplifier is divided into two two main groups. In Class B1, sometimes called *quiescent push–pull*, no grid current is allowed to flow, whereas in Class B2 the grid is allowed to go positive for at least part of each cycle. The latter type has a high percentage of odd harmonic distortion which is often a maximum at fairly low output levels, but this disadvantage is compensated by a high anode efficiency. However, the Class B2 is expensive since the driver valve, with the two output valves, forms an integral part of the stage, and together provide a sensitivity only of the same order as that of a single pentode.

It is common practice to design push–pull amplifiers for maximum power output without giving much consideration to odd harmonics, and if the resulting distortion is objectionable an improvement is made by increasing the load at the expense of power output. In this case all that is required is a single charac-

teristic curve of one valve, as is drawn in Fig. 4.5, and a load line constructed on it from the knee of the curve to the point $V_0$.

Then, power output is given by:

$$P_0 = 0{\cdot}5I_{A(\max)}(V_0 - V_{A(\min)}). \tag{4.4}$$

If, however, it is required to determine the amount of distortion present, for any given load, it is necessary to draw the load

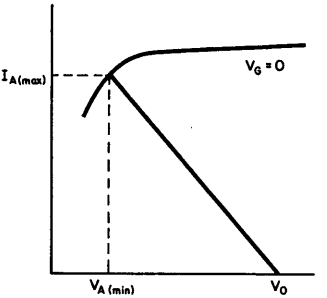



FIG. 4.5. Characteristic curve of one valve for the calculation of the power output of a Class B push–pull stage.

line on a complete characteristic, as shown in Fig. 4.6. One set of characteristic curves is inverted and placed below another set in such a way that the operating anode voltage on the $V_A$ axis of each set of curves is coincident and load lines are drawn having slopes representative of one-quarter of the anode to anode load.

*Design Steps*

1. Select a matched pair of valves.
2. Draw load lines on a composite characteristic and select the load which gives the best compromise between power output and distortion.
3. Calculate the turns ratio of the output transformer.
4. Determine the correct operating conditions for the screen grids.
5. Provide a suitable biasing arrangement.

DESIGN EXAMPLE 4.3

Required, a Class $B_1$ push–pull amplifier to provide a peak output power of 3·5 W.

A matched pair of EL85s is chosen and a composite characteristic drawn as in Fig. 4.6, with the operating anode voltage at 200 V. Two load lines are constructed, *AB*, having a slope of 0·25 mA/V, representing an anode to anode load of 16 kΩ, and *CD* representative of a 20 kΩ load.

From eqn. (4.4), the power outputs are respectively 3·85 W and 3·24 W. In fact, due to the presence of odd order harmonics,

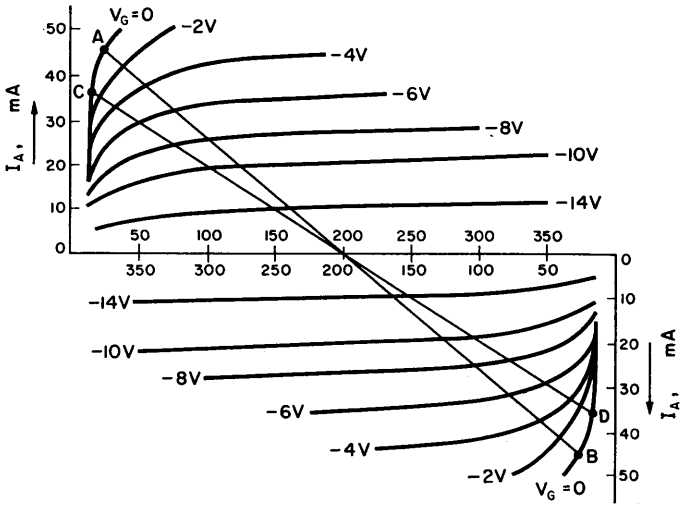



FIG. 4.6. Composite characteristic of a push–pull amplifier. The slope of the load lines represents a quarter of the equivalent resistance across the primary of the output transformer.

the power output will be somewhat greater than this, but if a valve is used having a low third harmonic characteristic the error will be small. Considering only the load line *AB*, harmonic distortion is of the order of 5% so a 16 kΩ load is suitable.

*Transformer turns ratio*, $n = \sqrt{(16000/3)} \doteqdot 74$. Thus, an output transformer is required having a step down ratio of 74 to 1, with the primary centre tapped for the provision of h.t. to the valve anodes.

*Biasing.* As the valves are to be biased to the point of cut-off, there will be no standing current which will permit the use of a cathode bias resistor. The bias voltage must therefore be obtained

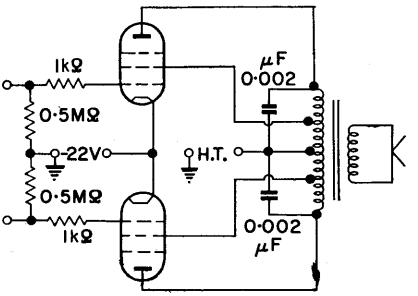



FIG. 4.7. Completed circuit of Design Example 4.3.

from a separate voltage supply. Examination of the $I_A/V_G$ characteristic shows that the required bias is $-22$ V and this will be applied between cathode and grid as shown in Fig. 4.7. The two grid resistors may be made 500 kΩ. Referring to the composite characteristic, it is noted that to obtain 3·8 W it is necessary to swing the grid voltage $\pm 22$ V about the operating point, so a drive of somewhat less than this is required from the preceding stage in order to obtain the specified output.

*Screen grid connection.* Although it is common practice to operate the screen grid at the same potential as the anode, it may also be connected to provide the so called "ultra-linear" output stage. In this case the screen grids are connected to tappings on the primary of the output transformer, at about 40% of the primary winding. This has the effect of reducing the amount of harmonic distortion present.[15]

*Parasitics.* At the point where each valve cuts off there is a high rate of change of current in the output transformer primary, and this may give rise to parasitic oscillations in the anode circuit. This may be largely overcome by connecting a capacitor across each half of the primary winding, 0·002–0·005 μF being the range of values used. When parasitics arise in the grid circuits, these may be stopped by means of grid stopper resistors or sometimes by a small capacitor between grid and cathode.

## 4.4. Transistor Power Amplifiers

The transistor is particularly well suited for use in power amplifier circuits. It is linear over practically the whole of its collector characteristic and is so efficient that it is almost possible to achieve the maximum theoretical efficiency of 50% for Class A and 78·5% for Class B amplifiers. The common emitter configuration is most widely used since it provides much greater power gain than the common collector arrangement. Its inherent distortion level is higher, but this can be largely compensated by the use of negative feedback.

### *The Class A Power Amplifier*

As in the valve case, the main steps in the design of such an amplifier are, the choice of operating point such that operation is restricted to the linear part of the characteristic, the biasing arrangement to obtain this operating point, and the determination of the correct load.

### *Design Considerations*

In a power amplifier there is very real danger of thermal runaway unless the biasing arrangement chosen is such as to prevent shift of the d.c. operating point. The circuit of Fig. 4.8 is widely used in this type of amplifier and will provide an acceptable degree of stability. The emitter resistor $R_E$ introduces voltage negative feedback and, in conjunction with the base

resistors $R_1$ and $R_2$, determines the value of the input voltage $V_{BE}$. An increase in emitter current causes a voltage drop across $R_E$ and reduces the base–emitter voltage. The base current is thus reduced, providing a large degree of compensation for the original change. If a stability factor is defined as $K = \delta I_{CEO}/\delta I_C$

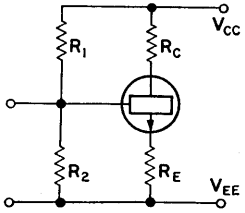



FIG. 4.8. Basic biasing arrangement of a transistor power amplifier stage.

(as in § 2.11), the minimum stability is obtained when $K$ is unity and the greater the value of $K$ the better the stability becomes. For the circuit of Fig. 4.8 this factor is:

$$K = 1 + \frac{\beta R_E}{R_E + R_B}, \tag{2.26}$$

if $R_E$ is large compared with $R_B$ (where $R_B = R_1R_2/(R_1 + R_2)$).

This equation shows that the greater the value of $R_E$ and the smaller the value of $R_B$, the higher will be the value of $K$ and hence the better the stability. The maximum value of $R_E$ depends on how much of the supply voltage can be dropped across it, and so how much voltage is available as signal swing in the collector resistor. Similarly, the minimum values for $R_1$ and $R_2$ depend on how much current may be drawn from the power supply by them. At very low values this potential divider will shunt the a.c. input. As a first step it is reasonable to make $R_B$ equal to $10R_E$ and then, using eqn. (2.26), to check the degree of stability obtained. In the design of this circuit, two other equations are required. Referring to Fig. 4.8,

$$V_B = V_{CC}R_2/(R_1 + R_2). \tag{4.5}$$

Also,

$$V_{BE} = V_B - I_E R_E, \tag{4.6}$$

from which,

$$V_B = R_E I_E + V_{BE}. \tag{4.7}$$

*Design Steps*

1. Select a suitable transistor.
2. Plot the load line on the output characteristic, select an operating point, and check distortion and power output.
3. With a knowledge of the minimum voltage to which the collector falls, choose a suitable value for $R_E$, to make $V_E$ a little less than $V_{C(\min)}$.
4. Using eqn. (2.26), determine the value of $R_B$ for the required stability factor.
5. Using eqns. (4.5) and (4.7), calculate the values of $R_1$ and $R_2$.
6. Select a suitable capacitor to decouple $R_E$.

DESIGN EXAMPLE 4.4

Required, an a.c. power of 0·75 W into a resistive load of 6·8 Ω, with low distortion and a stability factor of 8. A supply of −14 V is available.

To obtain an output with low distortion, a transistor is selected having a much greater power rating than the power actually

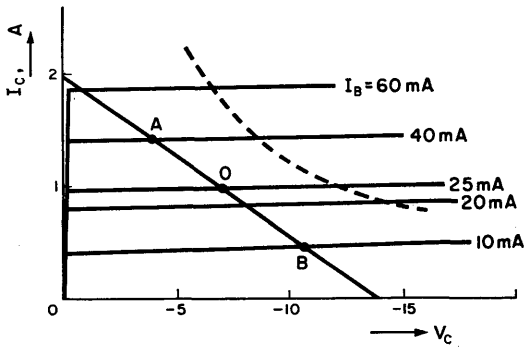



FIG. 4.9. Characteristic curves of an OC26 transistor.

required. Let it be an OC26 having a rating of 12·5 W at temperatures below 75°C, and whose output characteristic is given in Fig. 4.9.

*Load line.* With the load line as drawn, the operating point chosen is $V_C = -7$ V, $I_C = 1$ A, corresponding to an $I_B$ of 25 mA. For an input signal of 30 mA peak to peak, the output voltage varies between $-4$ and $-11$ V as the current swings through 0·95 A. Thus an output power of 0·83 W is obtained and the ratio $BO : AO = 1{\cdot}13$ indicates an acceptable distortion level.

*Emitter resistor.* Since $V_{C(\min)} = -4$ V and the standing anode current is 1 A, let $R_E = 3{\cdot}3\,\Omega$.

*Stability factor.* The transistor manufacturer gives $\beta = 33$ for an $I_C$ of 1 A. Substituting $\beta$ and $R_E$ in eqn. (2.26), for $K = 8$,

$$8 = 1 + \frac{33 \times 3{\cdot}3}{3{\cdot}3 + R_B},$$

therefore

$$7R_B = (33 \times 3{\cdot}3) - 23{\cdot}1,$$

so,

$$R_B = 12{\cdot}2\,\Omega.$$

*$R_1$ and $R_2$.*

$$V_E = I_E R_E \doteqdot V_B \quad \text{[from eqn. (4.7)]}.$$

But,

$$V_B = \frac{V_{CC}R_2}{R_1 + R_2} \quad \text{[from eqn. (4.5)]},$$

therefore

$$3{\cdot}3 = 14R_2/(R_1 + R_2),$$

from which

$$R_1 \doteqdot 3R_2.$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2},$$

therefore

$$12{\cdot}2 = \frac{3R_2^2}{4R_2} \quad \text{and} \quad R_2 \doteqdot 16\,\Omega.$$

Therefore

$$R_1 = 3R_2 = 48\,\Omega. \tag{4.8}$$

Let the values used be $R_1 = 47\,\Omega$ and $R_2 = 15\,\Omega$. The current drain due to $R_1$ and $R_2$ in series is 14 V/62 Ω ≒ 200 mA which is small compared with the standing current of the transistor.

The final circuit values are therefore $R_C = 6{\cdot}8\,\Omega$, $R_1 = 47\,\Omega$, $R_2 = 15\,\Omega$, and $R_E = 3{\cdot}3\,\Omega$. To obtain a reasonable low frequency response it would be necessary to make the emitter decoupling capacitor 1000 μF.

## 4.5. Audio Power Amplifier, Class A

### *Design Considerations*

The loudspeaker is coupled to the transistor by an output transformer and if the operating point is at the mid-point of the

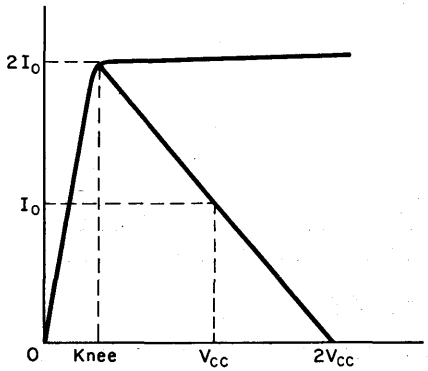



FIG. 4.10. Calculation of power output and load from a single collector characteristic. Note that for the purpose of illustration $V_{knee}$, normally less than 1 V, has been exaggerated with respect to $V_{CC}$. (See Fig. 4.11.)

dynamic collector load line, then it is possible for the collector voltage to swing between the knee voltage and twice the supply voltage, as shown in Fig. 4.10. The collector current swings from zero to twice the standing current. The load represented by this load line is therefore:

$$R_L = (V_{CC} - V_{\text{knee}})/I_0. \tag{4.9}$$

The maximum power output obtainable from this load is:

$$P_{0(\max)} = \frac{(V_{CC} - V_{\text{knee}})}{\sqrt{2}} \cdot \frac{I_0}{\sqrt{2}}. \tag{4.10}$$

Combining these two equations,

$$R_L = \frac{(V_{CC} - V_{\text{knee}})^2}{2P_{0(\max)}}. \tag{4.11}$$

These relationships may be used in the design of a power amplifier where a high degree of efficiency is required.

*Design Steps*

1. Allow for a slightly higher power than is actually required and, using eqn. (4.11), evaluate the required load $R_L$.
2. Determine the turns ratio of the transformer to match the speaker to this load.
3. Note the lowest voltage to which the collector swings and choose $R_E$ such that the voltage dropped across it is less than this voltage.
4. Making $R_B = 10R_E$, evaluate $R_1$ and $R_2$.
5. Choose a suitable capacitor with which to decouple $R_E$.

DESIGN EXAMPLE 4.5

A maximum output of 40 mW is required for a portable radio receiver using a supply voltage of 9 V.

*Choice of transistor.* Since the maximum theoretical efficiency obtainable is 50%, a transistor is chosen having a power rating

of 3 times the required power. The OC72 is such a transistor having a rating of 150 mW (when used with a heat sink) for temperatures below 30°C. From the collector characteristic of Fig. 4.11, the knee voltage is seen to be about 0·25 V.

*Choice of load.* In making use of eqn. (4.11) to evaluate the required load, allow for a power output of 45 mW. This will take account of loss in the ohmic resistance of the transformer

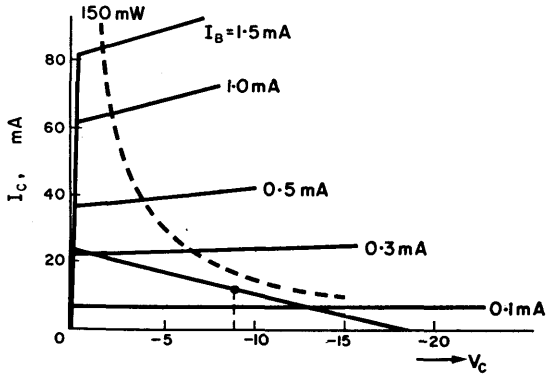



FIG. 4.11. Collector characteristic of an OC72. Note that the power dissipation curve is for the transistor when used with a heat sink.

primary, and also allow for the fact that the collector current cannot be taken down to zero because of leakage. In addition, to ensure that distortion is a minimum, consider the knee voltage to be 1·0 V. Then,

$$R_L = (9 - 1)^2/(2 \times 0{\cdot}045) = 700\ \Omega.$$

*Transformation ratio.* The transformer required to match a 3 Ω speaker to this load should have a turns ratio of $\sqrt{(700/3)}$ = 15·3 to 1.

*Emitter resistor $R_E$.* A load line for 700 Ω is now plotted on the output characteristic from the point $I_C = 0$, $V_C = 18$ V, and

the current at the operating point, $V_C = 9$ V, is seen to be 12·5 mA. If the current is allowed to swing from 23·5 mA down to 1·5 mA while the collector voltage swings from $-1{\cdot}5$ to $-16{\cdot}5$ V, an output of 42 mW is obtained. The emitter voltage may therefore be made 1·0 V.

Thus, $R_E = 1\text{ V}/12{\cdot}5\text{ mA} = 80\,\Omega$.
Make it 82 Ω which is a preferred value.
Now make $R_B = 820\,\Omega$ (i.e. $10R_E$),

$$V_B = R_2 V_{CC}/(R_1 + R_2) \doteqdot V_E.$$

Therefore

$$1{\cdot}0 = 9R_2/(R_1 + R_2) \quad \text{and} \quad R_1 = 8R_2,$$

but

$$R_B = R_1 R_2/(R_1 + R_2),$$

therefore

$$820 = 8R_2^2/9R_2.$$

This gives $R_2 = 920\,\Omega$ and $R_1 = 7360\,\Omega$, the nearest preferred values being 910 Ω and 7·5 kΩ. To complete the design a capacitor is chosen to decouple $R_E$. The reactance of a 250 μF capacitor at 60 c/s is approximately 10 Ω, which is satisfactory. The final design is therefore as shown in Fig. 4.12.

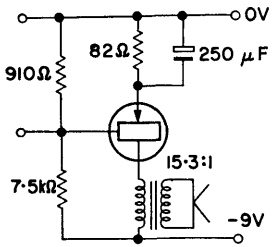



FIG. 4.12. Completed circuit of Design Example 4.5.

## 4.6. The Class B Push–Pull Amplifier

### *Design Considerations*

Theoretically, a Class *B* push–pull amplifier should have its two transistors biased to cut-off, but in practice this causes *cross-over distortion* if the change over in current from one

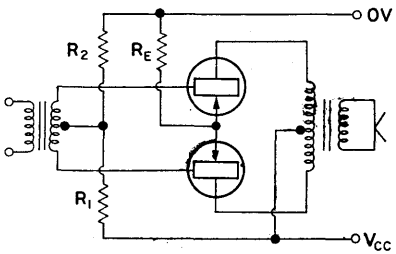



FIG. 4.13. Basic circuit of a Class B push–pull amplifier.

transistor to the other is not smooth. This type of distortion may be largely overcome by supplying the drive for the stage from a high resistance source and by applying a small forward bias to each transistor. The bias would typically be 100–200 mV giving rise to a quiescent current of a few milliamps. In the basic circuit of Fig. 4.13 the bias is provided by $R_1$ and $R_2$.

The value of $V_{BE}$ required at a transistor for any given collector current falls as the temperature rises, a decrease of 2·5 mV per °C being typical. The temperature range over which the stage is to be used should therefore be considered since, with an increase in temperature, $I_0$ rises and may reach such a magnitude that, in spite of the fixed bias provided, cross-over distortion is again present. Similarly, a large reduction in ambient temperature may so reduce the quiescent current that it becomes insufficient to reduce this distortion.

Such effects of temperature changes may be minimized by shunting $R_2$ with a negative temperature coefficient thermistor. Thus, as temperature rises, the resistance of the parallel combina-

tion falls and the base voltage $V_{BE}$ is decreased, offsetting the rise in collector current. A resistor in the emitter circuit $R_E$ similarly increases stability but as this is at the expense of efficiency it is usually of a low value.

The amount of power dissipated by the stage is dependent on the amplitude of the incoming signal and under no-signal conditions very little current is drawn from the supply source. The peak output power which the circuit can handle is a little less than 5 times the maximum collector dissipation of each transistor, and efficiencies of 70% may be readily achieved.

Assuming ideal transistors, the load presented to each collector is:

$$R_C = V_{CC}^2/2P_{O(\max)}. \tag{4.12}$$

However, in using this equation, a voltage somewhat less than $V_{CC}$ should be considered, allowing say 0·5 V to avoid distortion as the bottoming voltage is approached. Similarly, the value for $P_{O(\max)}$ should be higher than that required since the load on the transistor includes the unbypassed resistor $R_E$ and some power is lost in this resistor. The useful power output is given by

$$P_{\text{eff}} = P_{O(\max)} \cdot R_C/(R_C + R_E). \tag{4.13}$$

*Design Steps*

1. Select a suitable pair of matched transistors.
2. Using eqn. (4.12), evaluate the load to be presented to each collector and determine the ratio of the output transformer.
3. Select suitable values for $R_1$, $R_2$ and $R_E$ and check that with this value of $R_E$ the output power to the transformer is sufficient.

DESIGN EXAMPLE 4.6

Required, a Class B push–pull output stage giving a peak power output of 450 mW. A supply of 9 V is available.

*Transistors.* From the data sheets it is seen that an OC72 when used with a heat sink, may dissipate 130 mW at the collector

when used in ambient temperatures up to 35°C. Since the required output power is less than 5 times this figure a matched pair of transistors of this type will be suitable.

*Collector load.* In making use of eqn. (4.12), let $V_{CC}$ be reduced by 0·5 V and consider a total power output of 550 mW:

$$R_C = 72{\cdot}25/(2 \times 550 \times 10^{-3}) = 65{\cdot}7\,\Omega.$$

The collector to collector load is therefore $4 \times 65{\cdot}7\,\Omega = 262{\cdot}8\Omega$. The required transformer turns ratio for use with a speaker having a nominal impedance of 3 Ω is $\sqrt{(263/3)} = 9{\cdot}4$ to 1.

*Biasing.* Since the emitter resistor reduces efficiency its value is kept low; let it be the preferred value of 4·7 Ω. Checking the output, the total load on each transistor is

$$R_C + R_E = 65{\cdot}7 + 4{\cdot}7 = 70{\cdot}4\,\Omega.$$

Total power $P_{O(\max)} = V_{CC}^2/2(R_C + R_E) = 72{\cdot}25/140{\cdot}8 = 513\,\text{mW}$. Useful power output $= P_{O(\max)} \times R_C/(R_C + R_E) = 513 \times 0{\cdot}03 = 477$ mW, which meets the specification. The values of $R_1$ and $R_2$ are chosen bearing in mind the required bias voltage, let this be 150 mV, and the amount of current drain which may be permitted. Limiting the current drain to 1·5 mA, which is comparable to the quiescent current of the transistors, then,

$$R_1 + R_2 = V_{CC}/1{\cdot}5\,\text{mA} = 6\,\text{k}\Omega.$$

For $V_B = 150$ mV, $R_1 = 59R_2$. As this is not critical, and bearing in mind the spreads likely to be met in the transistors, let $R_1 = 5{\cdot}6$ kΩ and $R_2 = 100\,\Omega$.

For increased stability $R_2$ may be changed to a 220 Ω resistor shunted by an N.T.C. thermistor having a nominal resistance of 200 Ω.

Summing up the final design; turns ratio of output transformer 4·7 + 4·7 to 1, $R_E = 4{\cdot}7\,\Omega$, $R_1 = 5{\cdot}6$ kΩ, and $R_2 = 220\,\Omega$ shunted by an N.T.C. thermistor of 200 Ω.

CHAPTER 5

# Tuned Amplifiers

## Introduction

The tuned amplifier is used when it is required to amplify h.f. signals at one frequency, or band of frequencies, and reject others. A range of frequencies between 150 kc/s and 50 Mc/s is included in this category of amplifiers. Selectivity is obtained by the use of a parallel $L$–$C$ circuit which resonates at the desired frequency and which, at this frequency, has the high impedance necessary for the load of a voltage amplifier. The important characteristics of a tuned amplifier are the gain at resonance, the variation of gain with frequency in the immediate vicinity of resonance, and, if the frequency is to be varied, the way in which the gain changes when this is done.

## 5.1. The Parallel Tuned Circuit

In Fig. 5.1a a parallel tuned circuit is drawn, made up of an inductance $L$ having a resistance $r$, and shunted by a capacitance $C$.

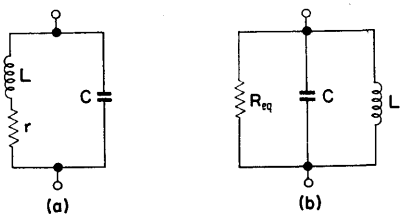



FIG. 5.1. Parallel tuned circuit with its resistive component (a) in series and (b) in parallel.

Resonance will occur when the capacitive and inductive reactances are equal, i.e. when $\omega_0 L = 1/\omega_0 C$, where $\omega_0 = 2\pi f_0$. From this, the resonant frequency

$$f_0 = \frac{1}{2\pi\sqrt{(LC)}}, \tag{5.1}$$

and the magnification

$$Q = \frac{\omega_0 L}{r} = \frac{1}{\omega_0 C r} = \frac{1}{r}\sqrt{\left(\frac{L}{C}\right)}. \tag{5.2}$$

The impedance of such a circuit may be written

$$Z(j\omega) = \frac{(r + j\omega L)/j\omega C}{r + j(\omega L - 1/\omega C)}, \tag{5.3}$$

and

$$Z(j\omega) = \frac{L/C}{r + j(\omega L - 1/\omega C)}$$

if $r$ is much less than $\omega L$. At resonance, when $\omega_0 L = 1/\omega_0 C$,

$$Z = \frac{L}{Cr} = R_D. \tag{5.4}$$

The impedance at resonance is purely resistive and is known as $R_D$, the *dynamic resistance*. The circuit of Fig. 5.1a may be redrawn as in Fig. 5.1b in which $C$ and $L$ are shunted by $R_{eq}$. The two circuits are equivalent at resonance provided that $R_{eq} = L/Cr$. From this, $r = L/CR_{eq}$ and if this is substituted in expression (5.2).

Magnification

$$Q = R_{eq}/\omega_0 L = \omega_0 C R_{eq} = R_{eq}\sqrt{\left(\frac{C}{L}\right)}. \tag{5.5}$$

## 5.2. Single Tuned Circuit Amplifier

A simplified circuit diagram is given in Fig. 5.2a, the coupling capacitor $C_C$ serving to prevent the valve 1 anode d.c. voltage appearing at the grid of valve 2. The equivalent network of this

circuit is as shown in Fig. 5.2b. $C$ represents the total circuit capacitance and includes the input capacitance of the second valve, and stray capacitance associated with wiring, etc., which together with $R_G$ (the input resistance of valve 2) are effectively

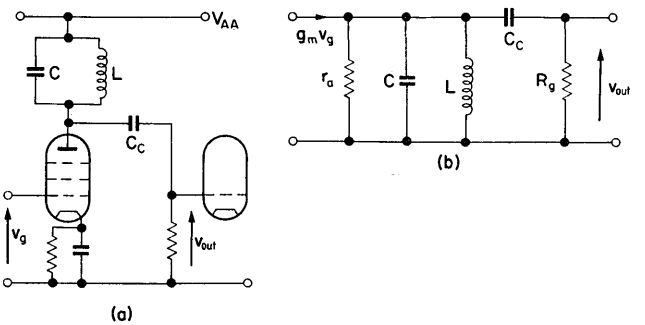



FIG. 5.2. Basic arrangement of a single tuned circuit amplifier with its equivalent network. $C_C$ is a blocking capacitor which keeps the $V_1$ anode voltage off the grid of $V_2$.

in parallel with the tuned circuit. The value of $C_C$ is chosen such that it has negligible reactance at the frequencies being amplified, and as it does not shunt the tuned circuit it may be neglected.

*Choice of Valve*

Examination of the equivalent network shows that the anode resistance of the valve is effectively in parallel with the tuned circuit load. A valve with a high $r_a$ is therefore required to prevent damping of the tuned circuit. As the impedance of the load will be high, large gains are possible and difficulties due to feedback may be encountered. Hence it is important that anode to grid capacitance be low if instability is to be avoided. In this frequency range the signal to be amplified will often be amplitude modulated. Because of the selectivity of the tuned circuit there will be no distortion of the modulation envelope, due to the presence of second harmonics resulting from curvature of the

valve characteristics. These considerations indicate that a pentode should be used.

Although the presence of second harmonics does not cause distortion, higher order harmonics may do so if there is a rapid change in the curvature of the $I_A/V_G$ curve. The danger of this is overcome by the use of a variable-mu-pentode, and such a valve is particularly suitable where some form of automatic gain control is required.

*Design Considerations*

The equivalent circuit is redrawn in Fig. 5.3, in which $R$ represents the total circuit resistance including $r_a$ of valve 1, the input resistance of valve 2, and the equivalent shunt loss resistance of $L$ and $C$.

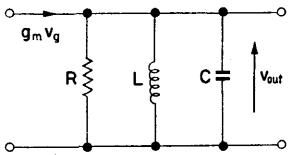



FIG. 5.3. Simplified equivalent network of the anode circuit of Fig. 5.2.

The impedance of the tuned circuit may be written,

$$Z(j\omega) = \frac{LR/C}{L/C + j(\omega LR - R/\omega C)}. \tag{5.6}$$

Let $d$, the dissipation factor equal $1/Q$, thus,

$$d = \frac{1}{\omega_0 CR} = \frac{\omega_0 L}{R} = \frac{1}{R}\sqrt{\left(\frac{L}{C}\right)}.$$

From eqn. (5.6),

$$Z(j\omega) = R\left\{\frac{(1/R^2)(L/C)}{(1/R^2)(L/C) + j[(\omega L/R) - (1/\omega CR)]}\right\}$$

$$= R\left\{\frac{d^2}{d^2 + jd(\omega LR/\omega_0 LR) - (\omega_0 CR/\omega CR)]}\right\},$$

therefore

$$Z = R\left\{\frac{d}{d + j[(f/f_0) - (f_0/f)]}\right\}, \tag{5.7}$$

where $f_0$ is the resonant frequency and $f$ is any other frequency.

The gain of the circuit from the grid of valve 1 to the grid of valve 2 is $g_m Z$, and is maximum at resonance when $Z = R$. At frequencies off resonance the impedance is less than $R$ and the gain is reduced as shown in Fig. 5.4.

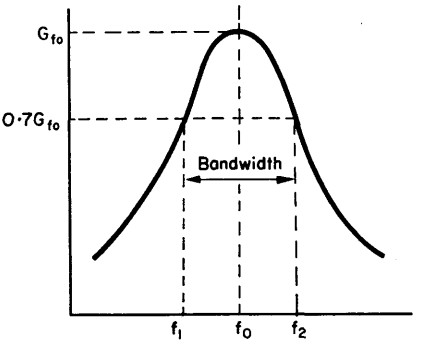



FIG. 5.4. Amplitude response of a single tuned circuit amplifier. The lower and upper 3 dB points are $f_1$ and $f_2$.

Let the bandwidth be defined as the range of frequencies between the two points at which the gain is 3 dB down, i.e. $1/\sqrt{2}$ times the gain at resonance. Referring to eqn. (5.7), this occurs when $(f/f_0) - (f_0/f) = \pm d$.

For circuits having a low dissipation factor $f$ will be close to $f_0$, and the gain is 3 dB down when

$$\frac{f^2 - f_0^2}{f_0^2} \doteqdot d,$$

and

$$\frac{f - f_0}{f_0} \cdot \frac{f + f_0}{f_0} = d.$$

To a close approximation

$$\frac{f+f_0}{f_0} = 2.$$

Hence, writing $\Delta f_0 = f - f_0$,

$$\frac{2\Delta f_0}{f_0} = d \quad \text{and} \quad \Delta f_0 = \frac{f_0 d}{2}.$$

The gain is therefore 3 dB down at the two frequencies

$$f_1 = f_0 - \frac{f_0 d}{2}, \quad f_2 = f_0 + \frac{f_0 d}{2}. \tag{5.8}$$

From these expressions,

$$d = \frac{f_2 - f_1}{f_0} = \frac{\text{bandwidth}}{f_0},$$

and since

$$d = \frac{1}{2\pi f_0 RC},$$

$$\text{bandwidth} = \frac{1}{2\pi RC} = \frac{f_0}{Q}. \tag{5.9}$$

For any circuit configuration, the gain-bandwidth product is a constant, it being possible to increase bandwidth at the expense of gain and vice versa. In the case of a single tuned circuit stage where gain $= g_m Z$ ($= g_m R$ at resonance),

$$\text{gain-bandwidth product} = g_m/2\pi C \quad \text{c/s}. \tag{5.10}$$

*Design Steps*

1. Select a suitable operating point, and determine the values of $R_K$ and $R_S$, the cathode and screen resistors.
2. Decouple $R_K$ and $R_S$.
3. For a given gain evaluate the necessary effective $R$.
4. Substitute this value of $R$ in eqn. (5.9) and thus determine

the capacitance required in order to obtain the correct bandwidth. By subtracting the sum of the stray capacitances from this, the value of the tuned circuit capacitor is obtained.

5. From eqn. (5.1) evaluate $L$ which, with $C$, will resonate at the desired frequency.
6. Calculate the dynamic resistance of this tuned circuit and determine what shunting resistance is required to provide the currect value of $R_{eff}$ as found in Step 1. To do this a typical coil resistance is assumed.

## Design Example 5.1

Required, an amplifier with a gain of 100 at a frequency of 200 kc/s. The bandwidth is to be 10 kc/s and the amplifier should be capable of handling a maximum input signal of 1 V peak to peak. A supply voltage of 250 V is available.

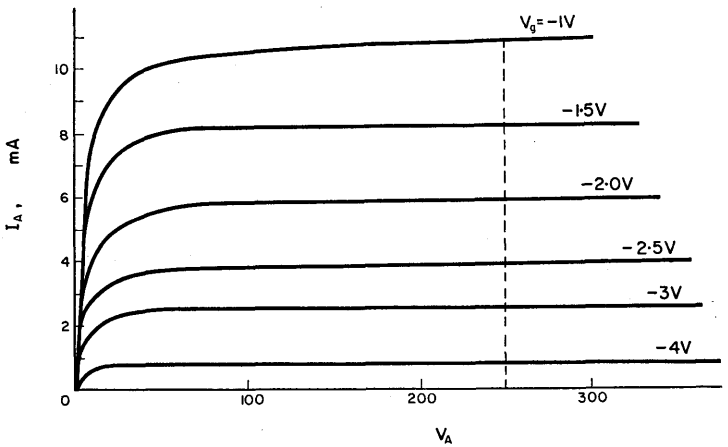



Fig. 5.5. Anode characteristics of a 6AU6 r.f. pentode.

Let the valve chosen be a 6AU6 r.f. pentode whose anode characteristics are given in Fig. 5.5, for a screen voltage of 150 V.

*Operating point.* Neglecting the ohmic resistance of the coil, which is small, the anode will have a standing voltage of the full h.t. of 250 V and a suitable operating point is at a grid voltage of $-1$ V. Under these conditions the standing anode current is 10·7 mA, the screen grid current is 4·3 mA, and (from the valve data sheets) $g_m = 5{\cdot}2$ mA/V and $r_a = 1$ MΩ.

Total current = 15 mA.
$R_K = 1$ V/15 mA = 66 Ω.
Power dissipated = $(15 \times 10^{-3})^2 \times 66 = 0{\cdot}225$ W.
Let $R_K$ be 68 Ω and 1 W.

At 200 kc/s a 0·1 μF capacitor has an impedance of less than 1 Ω, so this is suitable for decoupling $R_K$.

*Screen grid.*

$R_S = V_S/I_S = 150/(4{\cdot}3 \times 10^{-3}) = 35$ kΩ.
Power dissipated = $(4{\cdot}3 \times 10^{-3})^2 \times 35 \times 10^3 = 0{\cdot}65$ W.
Let $R_S$ be 33 kΩ and 1 W.

This resistor must also be decoupled and a 0·001 μF capacitor is suitable.

*Tuned circuit load.*

$$R_{\text{eff}} = \text{gain}/g_m = 100/(5{\cdot}2 \times 10^{-3}) = 19\ \text{k}\Omega.$$

From eqn. (5.9), bandwidth = $1/2\pi RC = 10$ kc/s.
Thus,

$$C = \frac{10^{-6}}{2\pi \times 19 \times 10} = 840\ \text{pF}.$$

Subtracting 25 pF for stray capacitance, tuned circuit capacitor $C = 815$ pF.

From eqn. (5.1),

$$L = \frac{1}{4\pi^2 f_0^2 C} = \frac{1}{40 \times 4 \times 10^{10} \times 840 \times 10^{-12}}.$$

Thus,

$$L = 744\ \mu\text{H}.$$

Assuming a typical coil resistance of 30 Ω,

$$R_D = \frac{L}{Cr} = \frac{744 \times 10^{-6}}{840 \times 10^{-12} \times 30} = 29{\cdot}5\ \text{k}\Omega,$$

and referring to the equivalent network of Fig. 5.2b this is in parallel with $r_a$ and $R_G$, each of 1 MΩ. The effective resistance is therefore approximately 28 kΩ.

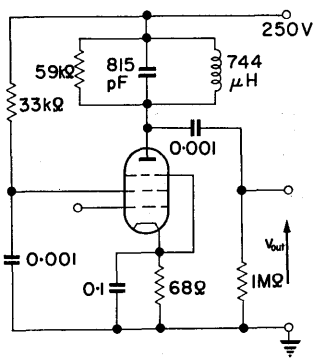



FIG. 5.6. Completed circuit of Design Example 5.1.

However, to satisfy the gain and bandwidth conditions it was earlier determined that $R_{\text{eff}}$ should be 19 kΩ. It is therefore necessary to shunt the tuned circuit with a resistor such that,

$$\frac{1}{R} = \frac{1}{19\ \text{k}\Omega} - \frac{1}{28\ \text{k}\Omega}, \quad \text{and} \quad R = 59\ \text{k}\Omega.$$

Let it be 56 kΩ.

*Coupling capacitor.* This is merely required as a blocking capacitor to keep the $V_1$ anode voltage off the grid of $V_2$. It should

have a reactance which is negligible at the frequency to be amplified. Again a 0·001 μF capacitor will be suitable. This completes the circuit, which is drawn in Fig. 5.6.

## 5.3. Tunable R.F. Amplifier with Constant Selectivity[16]

Where it is required that the frequency of an r.f. amplifier be tunable, it is usually desirable that, over the tuning range, the overall selectivity should remain constant.

The resonant frequency of a tuned circuit may be changed by varying either the inductance or the capacitance of the circuit. With permeability tuning, the inductance is varied by adjusting the position of an iron dust core within the coil. This produces less variation in selectivity and gain over the tuning range than does capacitor tuning, but is both more costly and more difficult to achieve. Capacitor tuning is therefore the more commonly used method, and with it special arrangements must be made in order to obtain constant selectivity.

### *Design Considerations*

In eqn. (5.9) the bandwidth of a parallel tuned circuit was given as

$$B = f_0/Q.$$

For constant selectivity, bandwidth should be constant and hence $Q$ should be proportional to $f_0$. Since $Q = \omega L/r$ it would appear that, with a fixed inductance having a given ohmic resistance, $Q$ is proportional to $f_0$. In fact as frequency increases the resistance of the coil also increases, and, particularly with iron-cored coils, $Q$ decreases as shown in Fig. 5.7. It is therefore necessary to make use of a network having a resistive component decreasing with frequency, which when added to the coil resistance will make the total resistance constant with frequency.

In Fig. 5.7, in which $r$ increases from 2 Ω to 10 Ω as $f$ increases from 400 kc/s to 1600 kc/s, there is needed a network whose resistance falls from 8 Ω to zero over the same frequency range causing the total resistance $R$ to remain constant at 10 Ω. Such

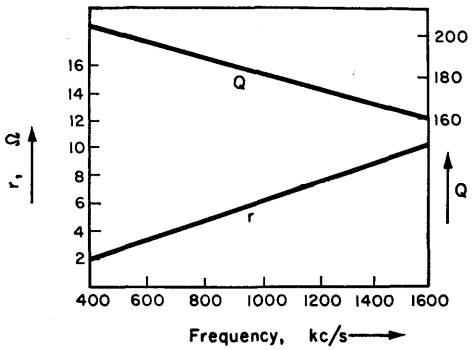



FIG. 5.7. The resistance and $Q$ of an inductance as a function of frequency.

a technique has the disadvantage that it derates the circuit performance at the lower frequencies, but the required network which is given in Fig. 5.8 is a simple one. Let the reactance of the $L$–$C$ arm be $X$.

Then

$$Z = \frac{jRX}{R + jX}$$

$$= \frac{RX^2 + jR^2X}{R^2 + X^2}.$$

Resistive component

$$R_1 = \frac{RX^2}{R^2 + X^2}. \tag{5.11}$$

Reactive component

$$X_1 = \frac{R^2X}{R^2 + X^2}. \tag{5.12}$$

The values of $L$ and $C$ may be chosen such that at the highest frequency in use the reactance is zero. Then, from eqn. (5.11), the resistive component $R_1$ is also zero. As the frequency decreases $X$ increases, and so therefore does $R_1$.

The network thus has the required characteristic and is used in series with the inductance of the amplifier tuned circuit. Its reactive component is usually small and may be neglected in comparison to the reactance of the coil itself.

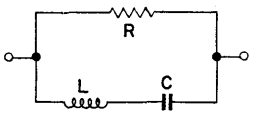



FIG. 5.8. Network used to obtain constant selectivity in a tuned circuit.

The impedance of the $L$–$C$ arm is:

$$jX = j\omega L - \frac{1}{j\omega C} = j\omega L\left(1 - \frac{1}{\omega^2 LC}\right). \qquad (5.13)$$

But from eqn. (5.11), $R_1 = 0$ when $X = 0$, that is at the resonant frequency of the network.

Then

$$\omega_0 L = \frac{1}{\omega_0 C} \quad \text{and} \quad \omega_0^2 LC = 1,$$

therefore

$$jX = j\omega L\left(1 - \frac{\omega_0^2 LC}{\omega^2 LC}\right) \quad \text{and} \quad X = \omega L\left(1 - \frac{f_0^2}{f^2}\right). \qquad (5.14)$$

Substituting in eqn. (5.11),

$$R_1 = \frac{R\{\omega L[1 - (f_0^2/f^2)]\}^2}{R^2 - \{\omega L[1 - (f_0^2/f^2)]\}^2}, \qquad (5.15)$$

and rearranging,

$$L^2 = \frac{R_1 R^2}{\omega^2 (R - R_1)\,[1 - (f_0^2/f^2)]^2}. \qquad (5.16)$$

There are three unknowns, $L$, $C$ and $R$, so values for $R_1$ are selected from Fig. 5.7 for three frequencies and substituted in the above equations.

*Design Steps*

1. Set up the correct bias conditions as in Design Example 5.1.
2. Calculate the maximum and minimum values of capacitance associated with the tuning capacitor and circuit, and thus determine the inductance for the frequency range to be covered.
3. Experimentally obtain the value of coil resistance over this range and plot a graph as in Fig. 5.7.
4. Select three frequencies at which selectivity compensation is to be applied and, at the two lower frequencies, note the values of $R_1$ required to make the total resistance, in each case, equal to the resistance of the coil at the highest frequency.
5. Substitute in eqns. (5.15) and (5.16) to determine values of $L$, $C$ and $R$ of the selectivity compensation network.

DESIGN EXAMPLE 5.2

Required, an amplifying stage covering the range 540–1600 kc/s with constant selectivity.

Using the 6AU6 pentode, the correct bias conditions can be set up as in Design Example 5.1.

*The tuned circuit.* A typical variable capacitor, with the stray capacitance of the circuit, will vary over a range of approximately 50–550 pF. With an inductance of 160 μH this gives a frequency coverage of 540–1800 kc/s which meets the specification.

If the resistance of this coil varies with frequency as is shown in Fig. 5.7, then at 1600 kc/s, $r = 10\,\Omega$ and $Q = \omega L/r = 160$. The compensation network must provide a resistive component such that the effective $R$ is $10\,\Omega$ and $Q = 160$ over the whole frequency range. In fact this will only be achieved accurately at

the three chosen frequencies but between these the error will be small. Let the chosen frequencies be 600, 1100 and 1600 kc/s.

At 600 kc/s, $r = 3{\cdot}4\,\Omega$ and required $R_1 = 6{\cdot}6\,\Omega$.

At 1100 kc/s, $r = 6{\cdot}7\,\Omega$ and required $R_1 = 3{\cdot}3\,\Omega$.

At 1600 kc/s, $r = 10\,\Omega$ and required $R_1 = 0$.

This latter condition is obtained at resonance, so $f_0 = 1600$ kc/s.

*$f = 1100$ kc/s.*

$$R_1 = 3{\cdot}3\,\Omega \quad \text{and} \quad f_0^2/f^2 = 2{\cdot}11.$$

Substituting in eqn. (5.16),

$$L^2 = \frac{3{\cdot}3R^2 \times 10^{-12}}{59{\cdot}5R - 196{\cdot}4}\ \text{H}. \tag{5.17}$$

*$f = 600$ kc/s.*

$$R_1 = 6{\cdot}6\,\Omega, \quad \omega L = 3768 \times 10^3 L \quad \text{and} \quad f_0^2/f^2 = 7{\cdot}1,$$

therefore

$$\left[\omega L\left(1 - \frac{f_0^2}{f^2}\right)\right]^2 = 37{\cdot}2\omega^2 L^2 = \frac{1768R^2}{59{\cdot}5R - 196{\cdot}4}, \tag{5.18}$$

and substituting this in eqn. (5.15) and solving, gives that $R = 7{\cdot}5\,\Omega$.

Hence, from eqn. (5.17), $L = 0{\cdot}86\ \mu$H.

Also at the resonant frequency of 1600 kc/s, $C = 1/\omega_0^2 L = 0{\cdot}01135\ \mu$F.

In the completed circuit of Fig. 5.9, the tuning capacitor is taken to earth instead of actually shunting the coil and compensating network. Consideration of an equivalent circuit shows that as far as the signal is concerned the capacitor serves the same purpose when connected in this manner. There is also the advantage that hand capacity effects are avoided.

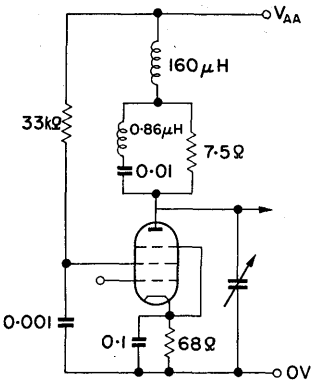



FIG. 5.9. Completed circuit of Design Example 5.2 to provide a tunable stage with constant selectivity.

## 5.4. CASCADED SINGLE TUNED AMPLIFIERS

The gain-bandwidth product of an amplifying stage is a figure of merit by means of which different circuit configurations may be compared. The product is a constant for a given circuit such that bandwidth may only be increased at the expense of gain. At broadcast frequencies this imposes very little limitation on design since the bandwidths in use are normally less than 10 kc/s, and for stability reasons a gain of 150 is rarely exceeded in a single stage.

At much higher frequencies however bandwidths of the order of several megacycles per second are sometimes required and the gain of a single stage is consequently restricted. In order to obtain a specified gain it is therefore often necessary to use more than one stage of amplification.

When a number of identical stages are used in cascade the figure of merit for the complete amplifier is not over-all gain times over-all bandwidth, but rather (over-all gain)$^{1/n}$ × over-all bandwidth, where $n$ is the number of stages.[3] As the number of stages is increased the over-all bandwidth decreases and, as

an approximation,

$$\text{Over-all bandwidth} = \frac{\text{Single stage bandwidth}}{1{\cdot}2\sqrt{n}}. \quad (5.19)$$

The gain-bandwidth product thus becomes:

$$G^{1/n}B_n = \frac{g_m}{2\pi C} \cdot \frac{1}{1{\cdot}2\sqrt{n}}, \quad (5.20)$$

so that,

$$B_n = \frac{g_m}{2\pi C} \cdot \frac{1}{1{\cdot}2\sqrt{n}} \cdot \frac{1}{G^{1/n}}. \quad (5.21)$$

Differentiating with respect to $n$ and equating to zero gives that

$$B_n \text{ is maximum when } n = 2\log_e G.$$

Therefore

$$G = e^{n/2}, \quad \text{and} \quad G^{1/n} = e^{1/2} = 1{\cdot}65.$$

This means that for an amplifier of this type, with a given over-all gain, maximum bandwidth is obtained when the individual stage gain is 1·65 (or 4·34 dB).

EXAMPLE. Using the 6AU6 pentode of Design Example 5.1, let the requirement be a 30 Mc/s amplifier with an over-all gain of 70 dB and with maximum bandwidth.

If the stray capacitance is 25 pF (as before), then the required inductance is 1·1 μH and no tuned circuit capacitor is needed.

Number of stages = 70/4·34 = 16.

$$G^{1/n}B_n = \frac{g_m}{2\pi C} \cdot \frac{1}{1{\cdot}2\sqrt{n}} = 6{\cdot}9 \text{ Mc/s}.$$

Therefore, bandwidth = 6·9/1·65 = 4·2 Mc/s.

An increase in the number of stages beyond 16 will cause reduction in bandwidth. This example illustrates the importance of considering the gain-bandwidth product when designing multi-stage tuned amplifiers. However, valves are available which would provide a gain-bandwidth of this magnitude with far fewer stages. Such a valve is the E810F wideband pentode which has

a $g_m$ of 50 mA/V. Since gain-bandwidth $= g_m/2\pi C$ this valve, in a single tuned stage, is capable of providing approximately 300 Mc/s and only two stages of amplification are required to obtain the same result. Thus, over-all gain = 70 dB = 3162, so gain per stage $= \sqrt{3162} = 57$. Similarly, over-all bandwidth = 4·2 Mc/s, so single stage bandwidth $= 1{\cdot}2\sqrt{2} \times 4{\cdot}2 = 7$ Mc/s.

## 5.5. Staggered Tuned Amplifiers

In eqn. (5.7) the impedance of a parallel tuned circuit was given as:

$$Z = R \cdot \frac{d}{d + j[(f/f_0) - (f_0/f)]}.$$

Since,

$$\frac{f}{f_0} - \frac{f_0}{f} \doteqdot 2\,\frac{f - f_0}{f_0}, \quad \text{and} \quad d = \frac{B}{f_0},$$

$$Z = R \cdot \frac{B/2}{B/2 + jx},$$

where $x = f - f_0$, the frequency off resonance. Then making $B = 2$ gives

$$\frac{Z}{R} = \frac{1}{1 + jx}, \tag{5.22}$$

$$\left|\frac{Z}{R}\right| = \frac{1}{\sqrt{(1 + x^2)}}. \tag{5.23}$$

This is the equation of the normalized selectivity curve of Fig. 5.10 and from it the frequency response of any parallel tuned circuit may be obtained.

Equation (5.23) may be written as $1/\sqrt{(1 + x^{2n})}$, so that the normalized selectivity curve represents the case of $n = 1$. The way in which the value of $n$ modifies the shape of the response is shown in Fig. 5.11. As $n$ increases, the 3 dB bandwidth remains

constant but the response flattens, and the cut-off outside the passband becomes sharper.

By means of Butterworth's technique,[3] it can be shown that each of these responses may be synthesized by a number of staggered tuned stages as indicated in Table 5.1, where $b$ is the bandwidth of a single stage.

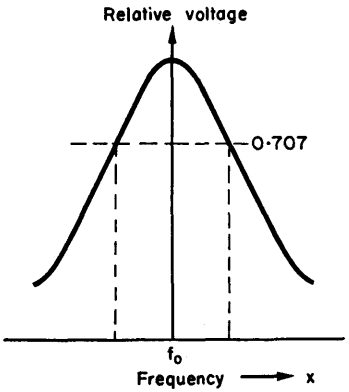



FIG. 5.10. Normalized selectivity curve $\left(\left|\frac{Z}{R}\right| = \frac{1}{\sqrt{(1-x^2)}}\right)$.

TABLE 5.1. STAGGERED TUNED STAGES TO PROVIDE BANDWIDTH $B$ AT FREQUENCY $f_0$

| $n$ | Single tuned stages required |
|---|---|
| 2 | Two stages at $f_0 \pm 0{\cdot}35B$, each having $b = 0{\cdot}71B$ |
| 3 | Two stages at $f_0 \pm 0{\cdot}43B$, each having $b = 0{\cdot}5B$ |
| | One stage at $f_0$ and $b = B$. |
| 4 | Two stages at $f_0 \pm 0{\cdot}46B$, each having $b = 0{\cdot}38B$ |
| | Two stages at $f_0 \pm 0{\cdot}19B$, each having $b = 0{\cdot}92B$ |
| 5 | Two stages at $f_0 \pm 0{\cdot}48B$, each having $b = 0{\cdot}31B$ |
| | Two stages at $f_0 \pm 0{\cdot}29B$, each having $b = 0{\cdot}81B$ |
| | One stage at $f_0$ and $b = B$ |

It will be noticed that most single stage bandwidths are less than the over-all bandwidth. A better over-all gain-bandwidth product is therefore obtainable than with cascaded synchronous

circuits. It is for this reason, together with the sharper cut-off outside the passband, that staggered circuits are used.

EXAMPLE. Required, an amplifier having a response of the form $1/\sqrt{(1 + x^6)}$, $(n = 3)$, at a frequency of 50 Mc/s and bandwidth of 6 Mc/s. Over-all gain to be 100 dB.

Since $n = 3$, from Table 5.1, there is required:

(a) a stage at 50 Mc/s with $b = 6$ Mc/s;
(b) a stage at $f_0 + 0{\cdot}43B = 52{\cdot}78$ Mc/s with $b = 3$ Mc/s;
(c) a stage at $f_0 - 0{\cdot}43B = 47{\cdot}22$ Mc/s with $b = 3$ Mc/s.

$$\text{Gain per stage} \doteqdot 33 \text{ dB} \doteqdot 45.$$

The gain-bandwidth products of the three stages are therefore 270 Mc/s for (a) and 135 Mc/s for (b) and (c).

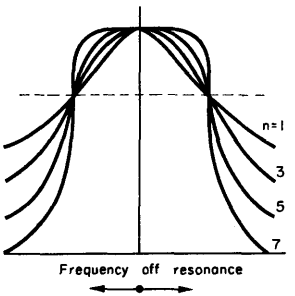



FIG. 5.11. $\left|\frac{Z}{R}\right| = \frac{1}{\sqrt{(1 + x^{2n})}}$ plotted for various values of $n$.

From eqn. (5.10) gain-bandwidth product $= g_m/2\pi C$, which is greatest for stage (a). Hence allowing 25 pF, the required $g_m$ is

$$g_m = 270 \times 10^6 \times 2\pi \times 25 \times 10^{-12} = 42 \text{ mA/V}.$$

The E810F pentode having a $g_m$ of 50 mA/V is therefore a suitable valve. The detailed design of each stage is carried out as in Design Example 5.1.

## 5.6. Double Tuned Circuits

Doubled tuned circuits are employed where a passband is required centered on a fixed frequency, and coupling between the two circuits may be inductive, capacitive or a combination of both. The most common type is that of inductive coupling as is used, for instance, in the intermediate frequency section of a superhet radio receiver. Only this method of coupling is therefore considered.

### *Inductively Coupled Circuits*

Inductively coupled circuits can be represented by the equivalent circuit of Fig. 5.12, in which $Z_1$ is the primary impedance, $Z_2$ is the secondary impedance and $M = k\sqrt{(L_1L_2)}$ is the mutual

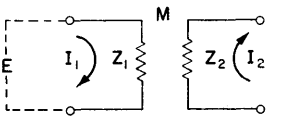



FIG. 5.12. Equivalent networks of an inductively coupled circuit.

inductance that exists between them. The performance of the circuit may be examined as follows:

Impedance coupled from secondary into primary $= (\omega M)^2/Z_2$. (5.24)

Equivalent primary impedance $= Z_1 + (\omega M)^2/Z_2$. (5.25)

$$\text{Primary current } I_1 = \frac{V}{Z_1 + (\omega M)^2/Z_2}. \tag{5.26}$$

Voltage induced in secondary $= -j\omega MI_1$. (5.27)

$$\text{Secondary current } I_2 = \frac{-j\omega MI_1}{Z_2} = \frac{-j\omega MV}{Z_1Z_2 + (\omega M)^2}. \tag{5.28}$$

When the mutual inductance is small, and the secondary impedance is large, the coupled impedance is small. Under these conditions the primary current is almost the same as if no secondary were present. If, however, $Z_2$ is small and $M$ is not small, then the coupled impedance is significant. When $Z_2$ is reactive with a given phase angle, the coupled impedance has the same phase angle but with the sign reversed. When $Z_2$ is purely resistive the coupled impedance is also resistive.

*Two Resonant Circuits, Inductively Coupled*

The behaviour of a pair of inductively coupled circuits, resonant at the same frequency, is largely determined by the degree of coupling between them. In Fig. 5.13 is shown the way primary and secondary currents vary with frequency for four values of $k$, the coefficient of coupling.

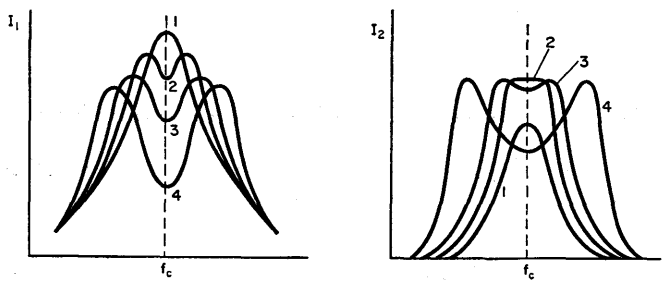



FIG. 5.13. Primary and secondary responses of inductively coupled tuned circuits for various coefficients of coupling.

Curve 1 represents a very small coefficient of coupling and both primary and secondary responses have approximately the same shape as would be obtained from single tuned circuits. If the coupling is increased until the coupled resistance, at resonance, is equal to the primary resistance, the response of curve 2 results. Such a coupling is known as the *critical* coefficient of coupling, and provides the maximum value of secondary current.

Thus, for critical coupling,

$$(\omega M)^2/R_2 = R_1. \tag{5.29}$$

Substituting $M = k\sqrt{(L_1L_2)}$ and rearranging gives

$$\text{Critical coefficient of coupling } k_c = 1/\sqrt{(Q_1Q_2)}. \tag{5.30}$$

If the coupling is increased beyond the critical value, as in curves 3 and 4, two humps appear in each response, and these become more pronounced and more widely spaced, the tighter the coupling is made. This is explained as follows. The secondary impedance is $R_2 + j[\omega L - (1/\omega C)]$, and the coupled impedance is $(\omega M)^2/\{R_2 + j[\omega L - (1/\omega C)]\}$. At resonance this is a maximum and is resistive and, since it is effectively in series with the primary impedance, the primary current at resonance is a minimum. At frequencies above and below resonance the secondary impedance is reactive, and the resulting coupled impedance is also reactive but of reversed sign. For instance an inductive reactance is coupled into the primary as a capacitive reactance. This neutralizes some of the primary reactance, lowering the primary impedance and increasing the primary current. Circuits which display this double humped effect are said to be overcoupled.

If the two tuned circuits have equal $Q$'s, the magnitudes of the humps are equal. If, however, $Q_1$ does not equal $Q_2$ and if the humps are widely spaced, the low frequency hump will tend to be the greater of the two.

*Design Considerations*

An equivalent circuit is given in Fig. 5.14 in which $R_1$ and $R_2$ represent the loading of the tuned circuits, including the $r_a$ of valve 1 and the input resistance of valve 2. The gain of the stage will be largely determined by the dynamic resistance of the tuned circuits and hence, for high gain, $L$ should be large compared with $C$. There is a limit however to the $L/C$ ratio which may be used, because for frequency stability reasons stray capacitance

should not form a large proportion of the total tuned circuit capacitance.

Since the circuit is to operate at a fixed centre frequency, it is important that no detuning should take place due to temperature

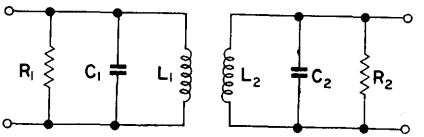



FIG. 5.14. Equivalent network of two inductively coupled tuned circuits, with the effects of loading represented by $R_1$ and $R_2$.

changes. Permeability tuning is therefore preferred, as this is more stable than capacitor tuning, and the tuned circuit capacitors are usually of the silvered mica type.

The development of design equations for the bandpass circuit is somewhat laborious, particularly for the general case of unequal $Q$'s, and so is not given here. For the special, and usual case of equal high $Q$'s with critical coupling, the relevant equations are as follows:

3 dB bandwidth of a single stage,

$$B = \frac{f_0\sqrt{2}}{Q} = \frac{\sqrt{2}}{2\pi RC}. \tag{5.31}$$

Single stage gain-bandwidth product,

$$GB = \frac{\sqrt{(2)}\, g_m}{4\pi C} \tag{5.32}$$

where

$$C = \sqrt{(C_1C_2)} \quad \text{and} \quad R = \sqrt{(R_1R_2)}.$$

Critical coefficient of coupling

$$k_c = 1/Q, \tag{5.33}$$

and combining eqns. (5.32) and (5.34),

$$k_c = \frac{B}{2\pi f_0}. \tag{5.34}$$

When $n$ circuits of this type are cascaded the overall bandwidth is less than a single stage bandwidth in the ratio

$$\frac{\text{Over-all bandwidth}}{\text{Single stage bandwidth}} = \frac{1}{1{\cdot}1\, n^{1/4}}. \qquad (5.35)$$

This expression is very accurate for a large $n$ and is within 10% of the correct value when $n = 2$.[3]

*Design Steps*

1. Estimate the stray capacitance associated with each tuned circuit and select a value for each fixed capacitor which will make $C = C_1 = C_2$.
2. Determine the value of inductance which will resonate with $C$ at the centre frequency.
3. Calculate the gain-bandwidth product of a single stage. If more than one stage is required to obtain the specified gain, use eqn. (5.35) to determine what bandwidth is necessary in each stage.
4. Substitute for $B$ in eqn. (5.31) thus obtaining the $Q$ for each circuit, and from eqn. (5.33) determine the critical coefficient of coupling.
5. Consider the effect of valve loading on the primary and secondary circuits, and evaluate the damping resistors if these are required.

DESIGN EXAMPLE 5.3 (Fig. 5.15)

Required, a bandpass amplifier having a centre frequency of 10 Mc/s and a bandwidth of 250 kc/s, gain to be at least 1500.

For a good gain-bandwidth product a valve with a high $g_m$ is necessary. Let the valve chosen be an EF183 r.f. pentode. This is a variable-mu valve which will permit the application of automatic gain control. From the data sheets for this valve, if $V_A = 200$ V, $V_S = 90$ V and $V_G = -2$ V, then $I_A = 12$ mA, $I_S = 4{\cdot}5$ mA, $g_m = 12{\cdot}5$ mA/V, $r_a = 500$ kΩ, and the input resistance at 40 Mc/s = 13 kΩ.

Let $C = C_1 = C_2 = 100$ pF (including stray capacitance). Single stage gain-bandwidth product

$$= \frac{\sqrt{(2)}\, g_m}{4\pi C} = \frac{1{\cdot}41 \times 12{\cdot}5 \times 10^{-3}}{12{\cdot}56 \times 100 \times 10^{-12}} = 14 \text{ Mc/s}.$$

Therefore,

$$\text{gain} = \frac{14 \times 10^6}{250 \times 10^3} = 56.$$

A gain of 1500 should therefore be obtainable with two stages. From eqn. (5.35), for an over-all bandwidth of 250 kc/s, single stage bandwidth (for $n = 2$) $= 1{\cdot}1 \times 2^{1/4} \times 250 \times 10^3 = 325$ kc/s.

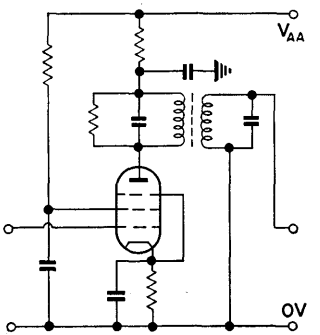



FIG. 5.15. Completed circuit of Design Example 5.3.

Checking gain with this new bandwidth, $GB = 14$ Mc/s, so gain per stage $= 14\,\text{M}\Omega/325\,\text{k}\Omega = 43$. Sufficient gain is still therefore available.

$$L = \frac{1}{4\pi^2 f_0^2 C} = \frac{1}{40 \times 10^{14} \times 10^{-10}} = 2{\cdot}5\ \mu\text{H}.$$

From eqn. (5.31) the required

$$Q = \frac{f_0\sqrt{2}}{B} = \frac{10 \times 10^6 \times 1{\cdot}41}{325 \times 10^3} = 43$$

and

$$k_c = 1/Q = 0{\cdot}023.$$

The primary tuned circuit is loaded by the $r_a$ of the valve, which is 500 kΩ. Similarly, the secondary of the first stage is loaded by $r_{g1}$ the input resistance of valve 2, which from the valve data sheets is 13 kΩ at 40 Mc/s. To obtain the value of $r_{g1}$ at 10 Mc/sec,

$$r_{g1}(f_1) = r_{g1}(f_2) \cdot \left[\frac{f_2}{f_1}\right]^2 = 13\ \text{k}\Omega \times \left[\frac{40}{10}\right]^2 = 208\ \text{k}\Omega.$$

From eqn. (5.31), the value of the effective damping resistance should be

$$R_{\text{eff}} = \frac{\sqrt{2}}{2\pi BC} = \frac{1{\cdot}41}{6{\cdot}28 \times 100 \times 10^{-12} \times 325 \times 10^3} = 6{\cdot}9\ \text{k}\Omega.$$

This must be the equivalent value of the damping resistor in parallel with the dynamic resistance of the tuned circuit and the valve loading resistance.

Assume that the transformer has primary and secondary $Q$'s of 100. Then,

$$R_D = Q\omega_0 L = 100 \times 6{\cdot}28 \times 10^7 \times 2{\cdot}5 \times 10^{-6} = 15{\cdot}7\ \text{k}\Omega.$$

The secondary winding is shunted by $r_{g1} = 208$ kΩ, giving an equivalent shunt resistance of $R_2 = 14{\cdot}6$ kΩ. To achieve the required $R_{\text{eff}} = 6{\cdot}9$ kΩ the damping resistor $R$ must be

$$R = \frac{R_s \cdot R_{\text{eff}}}{R_s - R_{\text{eff}}} = \frac{6{\cdot}9\ \text{k}\Omega \times 14{\cdot}6\ \text{k}\Omega}{14{\cdot}6\ \text{k}\Omega - 6{\cdot}9\ \text{k}\Omega} = 13\ \text{k}\Omega.$$

Similarly, the primary winding is shunted by the valve $r_a = 500$ kΩ, and the required primary damping resistor is 12·4 kΩ. Both damping resistors may therefore be made 12 kΩ.

*Decoupling.* The design values of $r_a$ and $g_m$ were selected for $V_A = 200$ V. Assuming an available h.t. supply of 250 V, the extra 50 V may be dropped in a decoupling resistor. Thus, $R = V/I = 50/(12 \times 10^{-3}) \doteqdot 4$ kΩ.

Let it be the preferred value of 4·7 kΩ. The decoupling capacitor should offer a signal path to earth which is small compared to this. At 10 Mc/s a 33 pF capacitor has a reactance of 483 Ω which is suitable.

The correct bias conditions are set up as in Design Example 5.1. In this example, the problem of unequal loading of the two tuned circuits has been easily overcome because the specification is not particularly stringent. In cases where the required $Q$'s are high, and where the relative values of $r_a$ and $r_{g1}$ are such as to give an unbalanced condition, a technique described by Langford-Smith[17] may be used. In this treatment a transformer is designed having equal values of primary and secondary $Q$ when unloaded. Designating them by $Q_{u1}$ and $Q_{u2}$ they should have such values that, when in circuit and loaded by $r_a$ and $r_{g1}$, $Q = \sqrt{(Q_{u1} \cdot Q_{u2})}$, where $Q$ is that required to provide the correct gain and bandwidth.

## 5.7. Tuned Amplifiers using Transistors

The necessary theory associated with parallel tuned circuits has been presented in §§ 5.1 and 5.6. Before proceeding with the design of transistor tuned amplifiers, the characteristics of transistors, when used at high frequencies, must first be studied.

### *Choice of Circuit Configuration*

The frequency response of a transistor may be expressed in terms of the frequency at which the current gain is reduced to $1/\sqrt{2}$ of its low frequency value. At this frequency the phase shift starts to change rapidly, and this can be of importance in obtaining stable amplification over a range of frequencies. The frequency at which this occurs is called the cut-off frequency and is denoted by $f_\alpha$ for the common base and $f_\beta$ for the common emitter configuration. To a rough approximation $f_\alpha = \beta f_\beta$, i.e. a higher cut-off frequency is obtainable with common base than with common emitter. Despite this fact, the common base arrangement is not necessarily preferred at high frequencies.

Transistors are available with sufficiently high values of $f_\beta$ that they may be used, in I.F. amplifiers for instance, in the common emitter configuration, taking advantage of the higher current gain of that circuit arrangement.

*High Frequency Equivalent Network*

At high frequencies the equivalent networks of Figs. 2.23 and 2.24 fail to yield accurate design results because of the h.f. effects that are inherent in the structure of a transistor. To take account of these effects the modified-$T$ and the hybrid-$\pi$ networks provide the most convenient representations for common base and common emitter respectively. These are shown in Fig. 5.16.

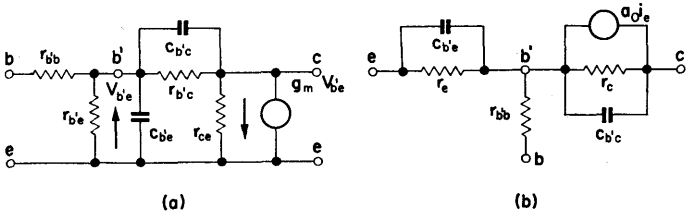



FIG. 5.16. The hybrid-$\pi$ and modified-$T$ equivalent networks for use at high frequency. The symbol $b'$ represents the internal base point.

As the last design example of this chapter will be a common emitter circuit, attention will be limited to the hybrid-$\pi$ network. The following relationships hold between the low frequency $T$ parameters of Fig. 2.23 and the hybrid-$\pi$ parameters:

$$r_{ce} = 2r_c(1 - \alpha), \quad r_{b'c} = 2r_c, \quad r_{b'e} = \frac{r_e}{(1 - \alpha)} + r_b - r_{bb'};$$

$$g_m = \frac{\alpha}{r_e + (r_b - r_{bb'})(1 - \alpha)} = \frac{g_m \cdot r_{b'e}}{1 - g_m \cdot r_{b'e}} = g_m \cdot r_{b'e}$$

$$\text{and} \quad c_{b'e} = \frac{\beta}{2\pi f_1 r_{b'e}}.$$

The symbols used have the following meanings:

$r_e$ is the emitter resistance, $r_b$ is the base resistance, and $r_c$ is the collector resistance.

$r_{bb'}$ represents the ohmic resistance which connects the active part of the base to the external base connector $b$.

$c_{b'e}$ is the emitter diffusion capacitance.

$r_{b'c}$ is the collector capacitance.

$f_1$ is the frequency at which the modulus of the common emitter forward current transfer ratio ($h_{fe}$) is unity, and

$\alpha$ and $\beta$ are the current gains for common base and common emitter.

Since $r_{b'e}$ is usually small the effect of $c_{b'e}$ is frequently negligible. The collector capacitance however is more significant since it shunts a medium to high resistance. This capacitance can seriously reduce bandwidth, and furthermore provides an internal feedback path from the collector output to the input. With good h.f. transistors $r_{b'c}$ and $r_{ce}$ will often be so large that they can be ignored. Ignoring $r_{ce}$ implies a load impedance which

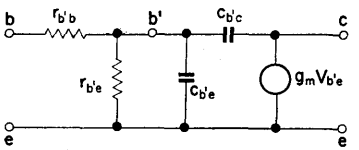



FIG. 5.17. Simplified hybrid-$\pi$ network.

is small compared with it, while $r_{b'c}$ may be ignored because at h.f. it is large compared with the reactance of $c_{b'c}$.

The hybrid $\pi$ of Fig. 5.16a may therefore often be reduced to the simplified network of Fig. 5.17.

## 5.8. NEUTRALIZATION[18]

As frequency increases, the reactance of $c_{b'c}$ falls, thus causing a feedback from output to input of the transistor. In most instances it is necessary to cancel the effects of this internal

feedback. The term unilateralization describes the process by which complete cancellation is obtained. A more realistic approach is that of neutralization in which only partial cancellation

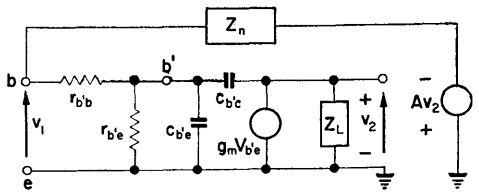



FIG. 5.18. Hybrid-$\pi$ equivalent network with external feedback.

is achieved, but this being sufficient to enable the effects of feedback to be ignored.

In Fig. 5.18 is shown a hybrid-$\pi$ equivalent circuit with a feedback network $Z_n$ fed with a signal derived from the output

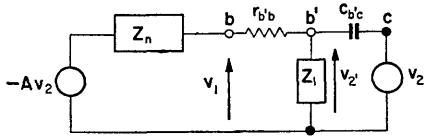



FIG. 5.19. Modification of Fig. 5.18 for the application of the superposition theorem.

voltage. For the cancellation of feedback effects, $v_1$ should be zero for any value of $v_2$. Employing superposition, $v_1$ may be written as the sum of two terms, one from $v_2$ and the other from the $Av_2$ generator. The circuit may be redrawn as in Fig. 5.19, in which

$$Z_1 = \frac{r_{b'e}}{1 + sC_{b'e}r_{b'e}},$$

$$v_2' \text{ (due to } v_2) = v_2 \frac{z_1}{Z_1 + 1/sC_{b'e}}.$$

Making use of Thevenin's theorem the circuit simplifies further to that of Fig. 5.20, in which

$$Z_2 = \frac{Z_1}{1 + sC_{b'c}Z_1}.$$

Using superposition,

$$v_1 \text{ (due to } v_2) = \left(\frac{Z_n}{Z_n + r_{bb'} + Z_2}\right)\left(\frac{Z_1}{Z_1 + 1/sc_{b'c}}\right)v_2,$$

$$v_1 \text{ (due to } Av_2) = -A\left(\frac{Z_2 + r_{bb'}}{Z_n + r_{bb'} + Z_2}\right)v_2,$$

therefore

$$v_1 = \left(\frac{Z_n}{Z_n + r_{bb'} + Z_2}\right)\left(\frac{Z_1}{Z_1 + 1/sc_{b'c}}\right)v_2$$

$$- A\left(\frac{Z_2 + r_{bb'}}{Z_n + r_{bb'} + Z_2}\right)v_2.$$

For

$$v_1 = 0, \quad \frac{Z_nZ_1}{Z_1 + 1/sc_{b'c}} = A(Z_2 + r_{bb'}).$$

Solving for $Z_n$ and substituting for $Z_1$ and $Z_2$ yields

$$Z_n = Ar_{bb'}\left(1 + \frac{c_{b'e}}{c_{b'c}}\right) + \frac{A}{sc_{b'c}}\left(1 + \frac{r_{bb'}}{r_{b'e}}\right). \qquad (5.36)$$

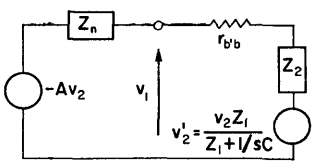



FIG. 5.20. The equivalent network further simplified by the use of Thevenin's theorem.

The required feedback compensation network is therefore a series $R$–$C$ circuit determined by the values of the transistor resistances and capacitances and by the feedback ratio $A$. For the capacitor, it is often a reasonable approximation to take its value as $C_{b'c}/A$. In many practical circuits, where the transistor is used at frequencies below $f_\beta$, the resistor is omitted and the capacitor alone provides adequate neutralization.

*Choice of Transistor*

The neutralizing network shunts both input and output impedance of the stage and its capacitive component forms part of the tuning capacitance. A transistor should therefore be chosen having a small value of $c_{b'c}$ and thus requiring a small feedback capacitor. It is also desirable that the component parts of the internal feedback path should not be subject to a very large spread. For operation in common-emitter mode, the transistor should have a common base cut-off frequency approximately 10 times the frequency at which the stage is to be operated.

*Design Considerations*

In the case of the valve bandpass amplifier, the design centred on a voltage amplifier having large input and output impedances, and the efficiency of power transference was largely ignored. With transistors the input and output impedances are comparatively small and hence the effect on the $Q$ of the tuned circuit is greater. Since these impedances are considerably different from each other, it is necessary that, in addition to providing the necessary bandwidth and selectivity, the tuned transformer should also act as an impedance matching device in order to achieve an efficient transference of power.

The circuit takes the form of Fig. 5.21, and the $Av_2$ term is obtained from the transformer secondary, so that $A$ is the transformation ratio. The collector is connected to a tap on the primary to reduce the loading effect which would otherwise occur

if the transistor output impedance was across the whole primary. This also enables the tuning capacitor to be of a reasonable value.

For maximum transference of power, the transformer should have a turns ratio,

$$n = \sqrt{\left(\frac{R_{out}}{R_{in}}\right)}, \tag{5.37}$$

where $R_{out}$ is the output resistance and $R_{in}$ is the input resistance of the next stage. To determine the value of the input and output impedances, use is made of the fact that, due to the neutralizing network, $v_2$ has no effect on $v_1$ and vice-versa. It is therefore permissible to short circuit $v_2$, and the input impedance is then

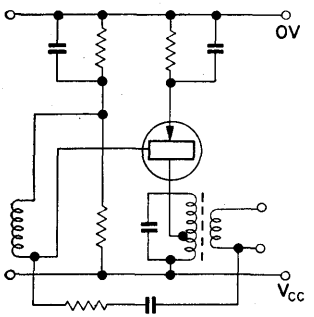



FIG. 5.21. Basic circuit of Design Example 5.4.

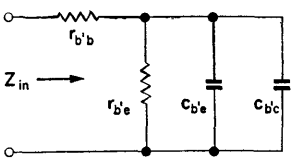



FIG. 5.22. Equivalent network of the input impedance of the neutralized i.f. amplifier stage.

formed by the circuit of Fig. 5.22. This may be resolved into a resistance $R_{in}$ and a capacitance $c_{in}$ in parallel. Similarly, by short circuiting $v_1$ the output impedance may be calculated, and the equivalent circuit redrawn as in Fig. 5.23.

This circuit may be further simplified by considering the shunting effects of the neutralizing circuit and then treating the input and output as two independent circuits. Thus, $R_n$ and $C_n$ may

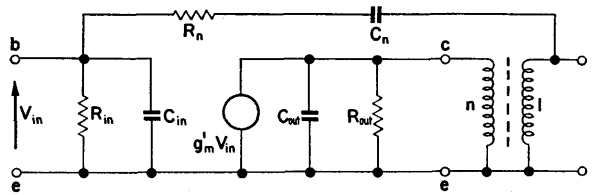



FIG. 5.23. Equivalent network to represent the output impedance of the stage.

be resolved into $R_p$ and $C_p$ in parallel across the input circuit, and also across the secondary of the output transformer. It appears as $n^2R_p$ and $C_p/n^2$ across the trasistor output impedance

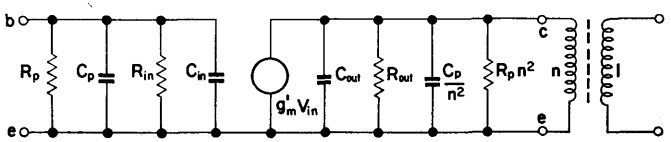



FIG. 5.24. Final equivalent network of the band pass amplifier of Fig. 5.21.

and obviously has less effect there than it does across the input circuit. The final equivalent circuit is therefore of the form of Fig. 5.24.

*Design Steps*

1. Decide under what d.c. conditions the transistor is to be operated, and calculate the values of emitter and base resistors and bypass capacitors in the usual way.
2. Draw a hybrid-$\pi$ equivalent circuit and calculate the value of $R_{out}$ and $R_{in}$, and thus determine the turns ratio $n$.
3. From eqn. (5.36) calculate $R_n$ and $C_n$ for the neutralizing circuit.

4. Calculate the equivalent impedance which represents the shunting effect of the neutralizing components across the input and output and construct the final equivalent circuit.
5. With the knowledge of the bandwidth required from each stage, use expression (5.9) to determine the tuned circuit effective $Q$.
6. Assume a value for the unloaded $Q$, select the tuned circuit capacitor $C$, calculate $L$ to resonate with $C$ at the centre frequency, and then determine the values of $r$, and $L/Cr$, the equivalent shunt resistor of the unloaded circuit.
7. Calculate the required shunting resistance across the tuned circuit to provide the correct bandwidth and thus establish what resistance should be reflected from the transistor output to achieve this.
8. Knowing this value, calculate at what point the transformer primary should be tapped.

DESIGN EXAMPLE 5.4

Required, a transistor I.F. amplifier to operate at a centre frequency of 470 kc/s.

From the makers data sheets, an OC45 has a typical $\alpha$ cut-off frequency of 6 Mc/s when operated at a collector voltage of $-6$ V and with an emitter current of 1 mA. This is more than 10 times the required centre frequency so this transistor is suitable. The circuit arrangement will be that of Fig. 5.21.

*Setting up the d.c. conditions.* Let $R_E$ be 820 Ω, so that $V_E = 0{\cdot}82$ V, with an emitter current of 1 mA. For a $V_C$ of $-6$ V, and allowing for $V_E$ and the voltage drop across the tuned circuit, $V_{CC} = -7$ V. Thus, making $V_B = -1$ V, $7R_2/(R_1 + R_2) = 1$ and $6R_2 = R_1$.

Also, make $R_1R_2/(R_1 + R_2) = 10R_E = 8{\cdot}2$ kΩ.

Therefore

$$R_1R_2 = 8{\cdot}2KR_1 + 8{\cdot}2KR_2.$$

$$6R_2^2 = 49{\cdot}2KR_2 + 8{\cdot}2\,KR_2 \quad \text{and} \quad 6R_2 = 57{\cdot}4\ \text{k}\Omega.$$

Let $R_2$ be 10 kΩ and hence $R_1$ should be 56 kΩ.

Suitable decoupling capacitors $C_E$ and $C_1$ are 0·25 μF and 0·1 μF respectively.

*Input and output impedances.* Based on Fig. 5.16a, and using values from the makers data sheets, the hybrid-π equivalent network is drawn as in Fig. 5.25a. In Fig. 5.25b is drawn the effec-

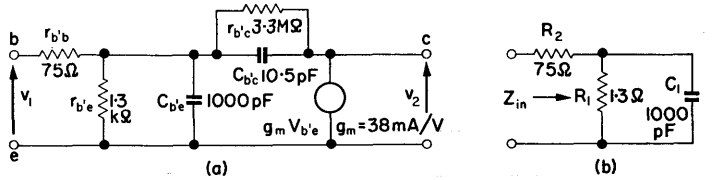



FIG. 5.25. Equivalent hybrid-π network of the circuit of Design Example 5.4 with an equivalent representation of the input impedance if $v_2$ is short circuited.

tive input circuit if $v_2$ is short circuited, and if $c_{b'c}$ and $r_{b'c}$ are ignored.

$$Z(R_1, C_1) = \frac{jR_1X_1}{R_1 + jX_1} = \frac{R_1X_1^2}{R_1^2 + X_1^2} + \frac{jR_1^2X_1}{R_1^2 + X_1^2}.$$

Substituting values this becomes a resistance of 78 Ω in series with a capacitive reactance of 310 Ω. Adding $r_{bb'} = 75\,\Omega$, $R_s = 153\,\Omega$ and $X_s = 310\,\Omega$.

This is now converted into an equivalent parallel circuit of $R_p$ and $C_p$.

Admittance

$$Y = G + jB = \frac{R_s}{R_s^2 + X_s^2} + \frac{jX_s}{R_s^2 + X_s^2},$$

therefore

$$R_P = \frac{R_s^2 + X_s^2}{R_s} \quad \text{and} \quad X_P = \frac{R_s^2 + X_s^2}{X_s}.$$

From which $R_p = R_{in} = 780\,\Omega$, and $X_p = 386\,\Omega$, so $C_p = C_{in} = 875$ pF. By short circuiting $v_1$ in Fig. 5.2 the output circuit becomes that of Fig. 5.26.

Making use of nodal analysis as discussed in Appendix A, at node $b'$,

$$\frac{v_1'}{Z_1} + \frac{v_1' - v_0}{Z_2} = 0; \tag{5.38}$$

at node $C$,

$$\frac{v_0}{Z_3} + \frac{v_0 - v_1'}{Z_2} + g_m v_1 = i_0. \tag{5.39}$$

From eqn. (5.38),

$$v_1' = Z_1 v_0/(Z_1 + Z_2).$$

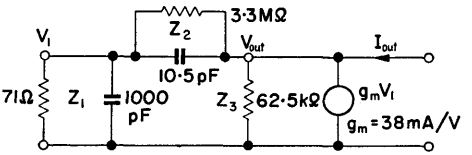



FIG. 5.26. Equivalent network of the output circuit, with $v_1$ of Fig. 5.25 short circuited.

Substituting in eqn. (5.39) and rearranging,

$$v_0\left[\frac{1}{Z_3} + \frac{1}{Z_2} + \left(\frac{Z_1}{Z_1 + Z_2}\right)\left(g_m - \frac{1}{Z_2}\right)\right] = i_0.$$

Therefore output impedance,

$$z_0 = \frac{v_0}{i_0} = \frac{1}{(1/Z_3) + (1/Z_2) + [Z_1(Z_1 + Z_2)]\,[g_m - (1/Z_2)]}.$$

Calculating the component parts of this expression separately yields:

$$Z_1 = (67{\cdot}9 - j14{\cdot}28); \quad 1/Z_1 = (14 + j2{\cdot}96)\,10^{-3}.$$

$$Z_2 = (0{\cdot}31 - j31{\cdot}8)\,10^3; \quad 1/Z_2 = (0{\cdot}3 + j31)\,10^{-6}.$$

$$Z_3 = 62{\cdot}5 \times 10^3; \quad 1/Z_3 = 16 \times 10^{-6}.$$

Thus, $$1/Z_3 + 1/Z_2 = (16{\cdot}3 + j31)\,10^{-6}.$$

$$Z_1/(Z_1 + Z_2) = (0{\cdot}474 + j2{\cdot}128)\,10^{-3}.$$

$$g_m - 1/Z_2 = (38{,}000 - j31)\,10^{-6}.$$

Substituting these values in eqn. (5.40),

$$Z_0 = \frac{(34{\cdot}4 - j111{\cdot}9)\,10^6}{13{,}705},$$

i.e. a resistance $R_s = 2{\cdot}51\ \text{k}\Omega$ in series with a reactance $X_s = 8{\cdot}16\ \text{k}\Omega$. Resolving into equivalent parallel components,

$$R_{\text{out}} = \frac{R^2 + X^2}{R} = 29\ \text{k}\Omega.$$

$$X_p = \frac{R^2 + X^2}{X} = 8{\cdot}16\ \text{k}\Omega, \quad \text{so} \quad C_{\text{out}} = 38\ \text{pF}.$$

*Transformer turns ratio.*

$$n = \sqrt{\left(\frac{29{,}000}{780}\right)} \doteqdot 6.$$

*Neutralizing circuit.*

$$R_n = Ar_{b'b}\left(1 + \frac{C_{b'e}}{C_{b'c}}\right) = 75/6\left(1 + \frac{1000}{10{\cdot}5}\right) = 1{\cdot}188\ \text{k}\Omega.$$

$$C_n = C_{b'c}/A = 6 \times 10{\cdot}5 = 63\ \text{pF}.$$

Let them be the preferred values of $1{\cdot}2\ \text{k}\Omega$ and 68 pF.

*Shunting effect on input.* At 470 kc/s the reactance of 68 pF $\doteqdot 5\ \text{k}\Omega$.

$$R_{pi} = \frac{R_n^2 + X_n^2}{R_n} = \frac{(1{\cdot}44 + 25)\,10^6}{1{\cdot}2 \times 10^3} = 22\ \text{k}\Omega,$$

$$X_{pi} = \frac{R^2 + X^2}{X} = \frac{26{\cdot}44 \times 10^6}{5 \times 10^3} = 5{\cdot}28\ \text{k}\Omega,$$

thus $C_{pi} = 64\ \text{pF}$.

*Shunting effect on output.*

$$R_{po} = n^2 R_{pi} = 792\ \text{k}\Omega.$$

$$C_{po} = C_{pi}/n^2 = 1{\cdot}8\ \text{pF}.$$

Assuming that the stage is followed by a similar stage having the same input impedance, the final equivalent circuit is that of Fig. 5.27. In this the conductance of the representative current

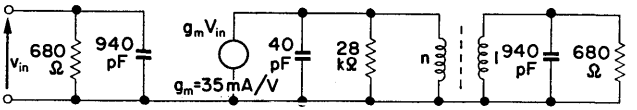



FIG. 5.27. Final equivalent circuit of Design Example 5.4. Note the different value of $g'_m$ to take account of the voltage drop in $r'_{bb}$.

generator has been given a value of 35 instead of 38 mA/V. This is necessary because the current is now shown as a function of $v_{in}$, at the base connection, and not of $v_{b'e}$. The difference in $g_m$ takes account of the voltage lost in $r_{bb'}$.

The capacitance reflected from the secondary into the primary of Fig. 5.26 is $940/n^2 = 26$ pF, giving a total primary capacitance of 66 pF. Similarly, the resistance reflected from the secondary into the primary is $680n^2 = 24{\cdot}5$ kΩ, giving a total shunt resistance of about 13 kΩ. To reduce the loading effect of this resistance on the tuned circuit, a tapped primary winding is used.

*The tuned primary.* Assuming that the complete I.F. amplifier is to consist of two stages, and that the over-all bandwidth is to be 7 kc/s, then each stage must have a bandwidth of $7 \times 1{\cdot}2\sqrt{2} \div 9$ kc/s.

From eqn. (5.9), bandwidth $= f_0/Q = 1/2\pi RC$, from which $Q_{eff} = 470/9 = 52$, and equivalent shunt resistance $R_{eq} = 70\,\text{k}\Omega$.

In circuits of this type, a transformer would be used having an unloaded primary $Q_u$ of 100, and tuned by a 250 pF capacitor.

To resonate with this capacitor at 470 kc/s, if the reflected capacitance from the transistor output is assumed to be negligible, $L = 450\ \mu H$.

Primary resistance $r = \omega L/Q_u = 13{\cdot}3\ \Omega$.

Equivalent shunt resistance $R_D = L/Cr \doteqdot 135\ k\Omega$.

It is therefore necessary that the resistance reflected from the transistor output across the primary should reduce the equivalent

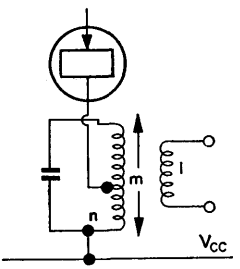



FIG. 5.28. Circuit to illustrate the auto-transformer action of the primary winding.

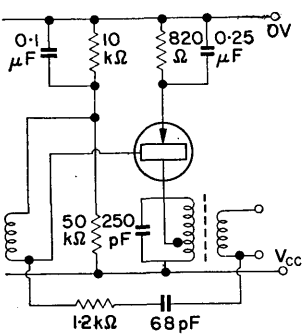



FIG. 5.29. Completed circuit of Design Example 5.4.

shunt resistance from 135 kΩ to the required value of 70 kΩ. The reflected resistance should thus appear as 145 kΩ and this is achieved by the auto-transformer action of the tapped primary

winding. Referring to Fig. 5.28, the output resistance of 13 kΩ across $n$ appears across the whole primary $m$ as 13 kΩ × $m^2/n^2$. For this to equal 145 kΩ, $m^2/n^2 = 11$ so that $m/n = 3{\cdot}3$. For matching purposes it has already been decided that $n : 1 = 6$, so the complete primary to secondary turns ratio becomes approximately 20: 1. The voltage gain of the circuit, measured from transistor input to transformer secondary output, is $g_m R/m$, thus,

$$\text{Gain} = 35 \times 70 \times 1/20 = 122.$$

The completed circuit of the first stage is given in Fig. 5.29. The second stage of the amplifier, which would normally be feeding into a detector circuit, would be modified to take account of the different input impedance of that circuit.

CHAPTER 6

# Zero Frequency Amplifiers

## Introduction

It is often required, particularly in control engineering problems, that an amplifier should amplify down to zero frequency. For a capacitor coupled amplifier this would require the use of an infinite capacitor. A zero frequency amplifier is able to amplify a change in d.c. level, as shown in Fig. 6.1.

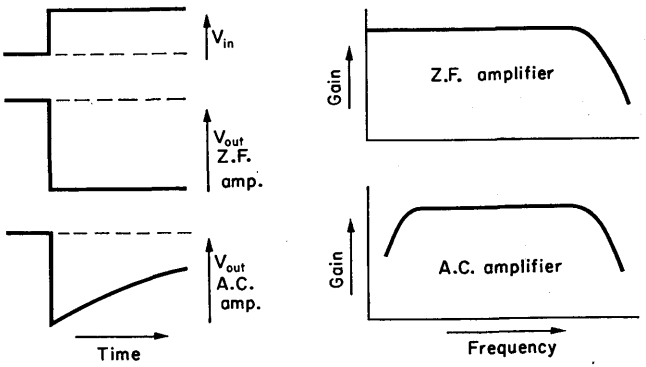



FIG. 6.1. Comparison of time and frequency responses of zero frequency and a.c. amplifiers.

## 6.1. AMPLIFIER TYPES

There are two general types of z.f. amplifiers:

(a) *Direct coupled.* One stage is coupled to the next either directly or by means of a resistance chain. Two such cir-

cuit arrangements using valves and transistors are given in Fig. 6.2.

(b) *Modulator (Chopper).* The input is chopped, amplified as an a.c. signal and reconstituted at the output, as shown in Fig. 6.3.

Type (a) will usually have a greater bandwidth than type (b) but the latter has less output drift.

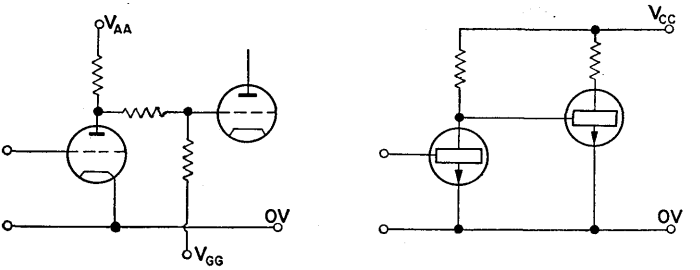



FIG. 6.2. Direct coupled amplifier stages. $V_{GG}$ is the negative voltage required to provide the correct bias for the second valve.

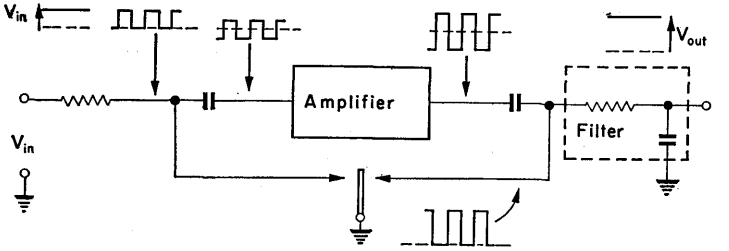



FIG. 6.3. Schematic diagram to illustrate the operation of a chopper z.f. amplifier. Chopping is achieved by means of a mechanical relay driven from an a.c. source. This could be replaced by a solid state switching device.

## *Drift*

With no input signal, the output from a z.f. amplifier can alter due to internal changes of operating conditions. These changes are amplified in the same way as input signals and cannot be

separated from them. The change in output voltage for zero input is known as drift. Drift is measured by shorting the input terminals and monitoring the output, and is typically given in volts per hour; so that different amplifiers may be compared, drift is usually referred to the input.

$$\text{Input drift } (V_{di}) = \frac{\text{output drift } (V_{do})}{\text{amplifier gain } (A)}. \tag{6.1}$$

Drift signals are of very low frequency having a period which may vary from several seconds to hours, and are consequently not passed by a.c. amplifiers.

*Zeroing*

Since the output level is of significance, with a z.f. amplifier, some means is required of setting the output to the required datum when the input is zero. (For example, see Fig. 6.6.)

## 6.2. Direct Coupled Amplifiers

The conventional common cathode amplifier is basically a d.c. amplifier.

*Gain*

The working point of a d.c. amplifier is a function of the input voltage, and the small signal gain is the same as for a capacitively coupled amplifier.

$$A = \frac{-\mu R_L}{r_a + R_L} = \frac{-g_m}{g_a + G_L}. \tag{6.2}$$

The small signal gain will vary with input signal because of the change in valve parameters with operating point. (See Fig. 6.4.)

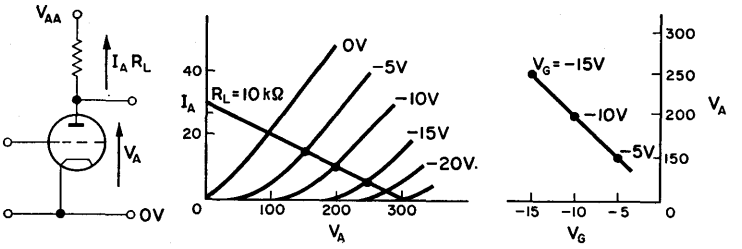



FIG. 6.4. Consideration of a single stage direct coupled amplifier to show how the anode voltage $V_A$ varies with the d.c. grid voltage $V_G$.

## DESIGN EXAMPLE 6.1

Required, a direct coupled amplifier providing a gain of 10 with signal inversion. The output voltage should be 150 V when the input voltage is zero.

$$\text{Gain } A = \frac{-\mu R_L}{r_a + R_L + (\mu + 1) R'_K} \text{ [from eqn. (1.12)].} \tag{6.3}$$

$R'_K$ is the effective value of cathode resistance, i.e. $R_K$ of Fig. 6.5 in parallel with $R_S$.

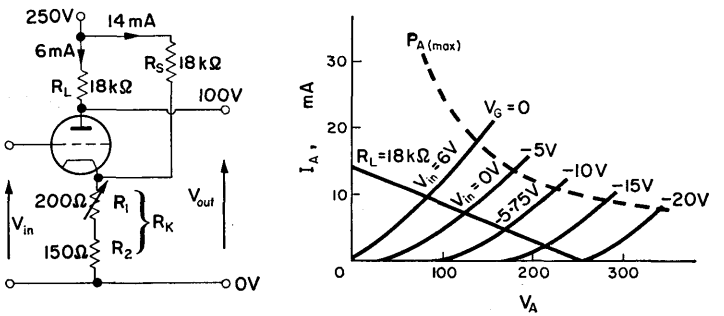



FIG. 6.5. Circuit diagram of Design Example 6.1.

*Valve.* One half of an ECC82 general purpose triode is suitable for this purpose having a typical $\mu$ of 20 and $r_a$ of 10 kΩ. Let the operating point be 150 V and 6 mA which requires a grid–cathode voltage of −5 V.

*Cathode resistance.* Following the method of § 1.6 let the total current through $R_K$ be 20 mA.

$$R_K = \frac{-V_{GK}}{I_{RK}} = \frac{5\text{ V}}{20\text{ mA}} = 250\,\Omega.$$

*Anode resistance.* Rearranging eqn. (6.3),

$$R_L = \frac{-A[r_a + (\mu + 1)\,R_K]}{\mu + A}. \tag{6.4}$$

Substituting the nominal values,

$$R_L = \frac{10(10\text{ k}\Omega + 5{\cdot}25\text{ k}\Omega)}{10} = 15{\cdot}25\text{ k}\Omega.$$

(Let it be 18 kΩ.)

*Supply voltage $V_{AA}$.* A loadline of 18 kΩ, drawn through the operating point of 150 V, 6 mA gives a supply voltage of 250 V.

*Bias current resistor $R_S$.* The voltage across $R_S$ is the supply voltage minus the cathode voltage.

$$R_S = \frac{V_{AA} - V_K}{I_R} = \frac{V_{AA} - V_K}{I_{RK} - I_A} \doteqdot \frac{250\text{ V}}{14\text{ mA}}, \tag{6.5}$$

$$\doteqdot 18\text{ k}\Omega.$$

*Zero control.* To enable the output voltage to be set to the required value, $R_K$ may be adjusted. Make $R_1$ a 200 Ω variable resistor and $R_2$, 150 Ω.

## 6.3. Pentode Amplifiers

Many pentodes can be operated with extremely large anode resistors and low screen grid voltages. In this manner stage gains of several hundred can be obtained although the bandwidth will be relatively small because of the large anode time constant.

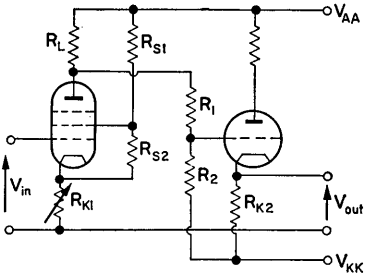



FIG. 6.6. Pentode amplifier with cathode follower output.

To prevent loading of the anode resistor, the cathode follower output circuit of Fig. 6.6 can be used.

A typical requirement is that the amplifier should give zero volts out for zero input volts and that the output should be able to move both positively and negatively. The amplifying valve requires negative grid volts which can be provided by a resistance chain from the anode supply line. If a cathode resistor is used, it will reduce the gain, but the negative feedback could be desirable in stabilizing it.

Once the anode voltage for zero output is found, the voltage divider for the cathode follower input can be designed. To prevent loading of $R_L$, $R_1 + R_2$ should be at least 5 times $R_L$. Loading of $R_L$ will reduce the gain (by reducing the effective load resistance), and the voltage swing (by drawing a current through $R_L$ even when $V_1$ is cutoff). If the loading is small, a sufficiently accurate relationship is:

$$\frac{R_2}{R_1 + R_2} = \frac{-V_{GG}}{V_A - V_{GG}}, \quad \text{where} \quad R_1 + R_2 \gg R_L.$$

*Determination of $R_{K2}$*

The fact that the output voltage is required to move both positively and negatively must be considered when selecting a value for $R_K$. Consider the circuit of Fig. 6.7a. When the valve is conducting,

$$I_A = I_R + I_L = \frac{(V_L - V_{KK})}{R_K} + I_L.$$

Let $I_{A(\max)}$ be the current supplied by the valve when the output voltage is maximum positive, $V_{L(\max)}$. Then the voltage across the valve is $V_{AA} - V_{L(\max)}$ and the maximum current the valve can supply is indicated on the valve characteristics at the intersection of $V_G = 0$ V and $V_A = (V_{AA} - V_L)$.

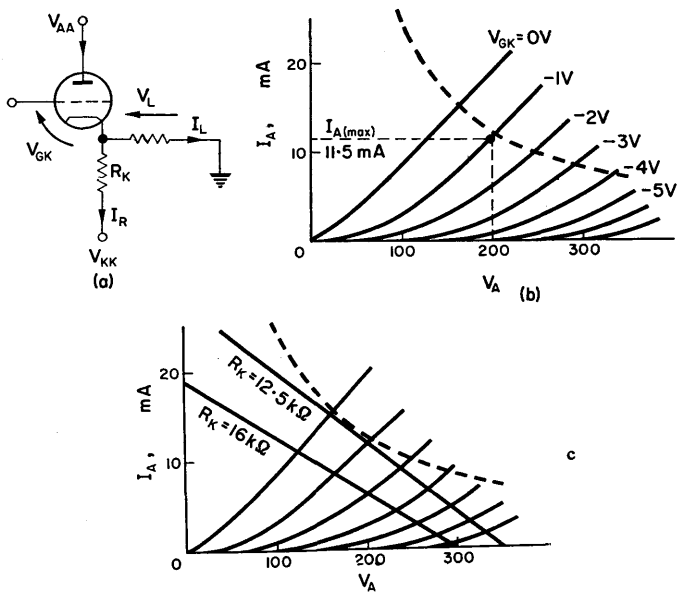



FIG. 6.7. Determination of the optimum value for $R_K$ in the cathode follower stage. In (c) the two load lines for $R'_K$ represent $R_K$ in parallel with $R_L$.

If the valve is an ECC81 double triode and the output voltage is required to be $\pm 50$ V into a load of 20 kΩ, then with $V_{AA} = 250$ V and $V_{KK} = -250$ V:

$$V_{L(\max)} = 50 \text{ V},$$

$$V_{A(\min)} = V_{AA} - V_{L(\max)} = 200 \text{ V}.$$

If the grid voltage $V_{GK} = -1$ V is accepted as a limit instead of $V_{GK} = 0$ V, then from Fig. 6.7b,

$$I_{A(\max)} = 11{\cdot}5 \text{ mA}.$$

The maximum load current,

$$I_{L(\max)} = \frac{V_{L(\max)}}{R_L} = \frac{50 \text{ V}}{20 \text{ k}\Omega} = 2{\cdot}5 \text{ mA},$$

$$R_K = \frac{\text{Voltage across } R_K}{\text{Current in } R_K} = \frac{V_{L(\max)} - V_{KK}}{I_{A(\max)} - I_{L(\max)}} \qquad (6.6)$$

$$= \frac{300 \text{ V}}{9 \text{ mA}} = 33{\cdot}3 \text{ k}\Omega.$$

This is the minimum value and, using it, the standing valve current

$$I_A \text{ (when } V_L = 0) \text{ is } I_{A1} = I_{K1} = \frac{250 \text{ V}}{33{\cdot}3 \text{ k}\Omega} = 7{\cdot}5 \text{ mA}.$$

When the valve is cut off, $I_A = 0$, then

$$R_K = \frac{V_{L(\min)} - V_{KK}}{I_{L(\max)}} \qquad (6.7)$$

$$= \frac{200 \text{ V}}{2{\cdot}5 \text{ mA}} = 80 \text{ k}\Omega.$$

This is the maximum value and gives rise to a standing valve current of

$$I_{A2} = I_{K2} = \frac{250 \text{ V}}{80 \text{ k}\Omega} = 3{\cdot}125 \text{ mA}.$$

In general, as the value of $R_K$ is increased, the standing anode current decreases, but at the same time the cathode follower efficiency decreases as the point of cut-off is approached. The load lines drawn in Fig. 6.7c represent the two values of $R_K$, each shunted by $R_L$. At $V_A = 250$ V (when $V_L = 0$) the bias voltages required are;

$$V_{GK1} = -2{\cdot}5\text{ V}, \quad \text{for} \quad R_K = 33\text{ k}\Omega,$$

$$V_{GK2} = -3{\cdot}7\text{ V}, \quad \text{for} \quad R_K = 80\text{ k}\Omega.$$

*Equivalent Network*

If in Fig. 6.8 $(R_1 + R_2)$ is much larger than $R_{L1}$, then the signal voltage across $R_{L1}$ is $-\mu_1 R_{L1} v_{in1}/(r'_{a1} + R_{L1})$, where $r'_{a1} = r_{a1} + R_K(\mu + 1)$.

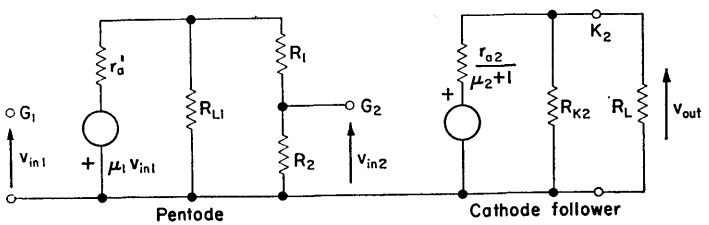



FIG. 6.8. Equivalent z.f. network of the circuit diagram of Fig. 6.6.

Then,

$$v_{in2} = \frac{-\mu_1 R_{L1}}{(r'_{a1} + R_{L1})} \cdot v_{in1} \cdot \frac{R_2}{(R_1 + R_2)}$$

and

$$v_{out} = \frac{[\mu_2/(\mu_2 + 1)]\,[R_L R_K/(R_L + R_K)]}{[r_{a2}/(\mu_2 + 1)] + [R_L R_K/(R_L + R_K)]} \cdot v_{in2}$$

$$= \frac{\mu_2 R_L R_K}{(\mu_2 + 1)\,R_L R_K + (R_L + R_K)\,r_{a2}} \cdot v_{in2}.$$

Voltage gain

$$= \frac{v_{out}}{v_{in1}} = \frac{-\mu_1 R_{L1}}{(r_{a1} + R_{L1})} \cdot \frac{R_2}{(R_1 + R_2)} \times$$

$$\times \frac{\mu_2 R_L R_K}{(\mu_2 + 1) R_L R_K + r_{a2}(R_L + R_K)}$$

$$= [A_1 R_2/(R_1 + R_2)] A_2, \qquad (6.8)$$

where $A_1$ is the gain of the pentode and $A_2$ is the gain of the cathode follower.

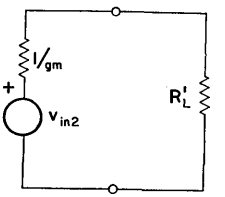



FIG. 6.9. Simplified equivalent network of a cathode follower. Since $R_L$, the effective load, will be much greater than $1/g_m$ the voltage gain will be approximately unity.

It is usually sufficient to regard the cathode follower as being represented by the equivalent circuit of Fig. 6.9 in which $R'_L$ is the effective load. Since $1/g_m$ is very much smaller than $R'_L$ the gain of such a stage is very nearly unity, i.e. $A_2 \doteqdot 1$.

DESIGN EXAMPLE 6.2

Required, an amplifier consisting of a pentode and cathode follower, to provide an output of $\pm 50$ V into a 20 kΩ load. The gain of the pentode should be the maximum practical value obtainable from an EF86 operating from a 250 V supply.

*The pentode circuit.* If resistive coupling is used, there will be a signal reduction of approximately one-third between the pentode and cathode follower, so a voltage swing of $\pm 80$ V is required at the anode.

Using the test circuit of Fig. 6.10a curves are plotted relating gain to screen grid voltage, with control grid voltage as parameter (Fig. 6.10b).

For each value of $V_{GK}$ another curve may be drawn, as in Fig. 6.10c, in which $V_A$ is plotted against $V_S$. Examination of

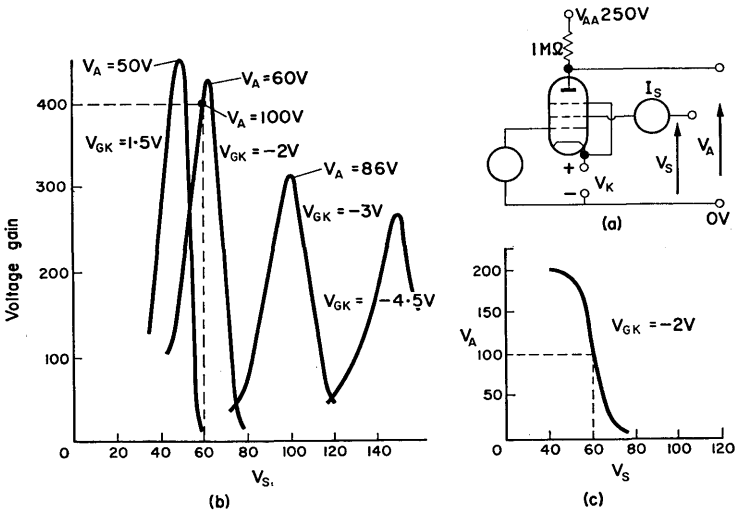



FIG. 6.10. Selection of operating conditions for a pentode amplifier.

these curves shows that a grid voltage of −2 V is a reasonable compromise between gain and possible anode voltage swing; a screen voltage of 60 V giving a gain of 400 and a standing anode voltage of 100 V.

*Anode load resistor.* The anode load resistor used in the test circuit has a value of 1 MΩ. A larger value would provide higher gain but the coupling network would reduce the effective value of this resistor, and thus reduce the maximum positive signal voltage swing. These considerations indicate that 1 MΩ is a suitable value.

*Screen grid voltage.* With $V_S = 60$ V and $V_A = 100$ V the measured screen current is 40 μA and the anode current 150 μA. For the screen supply the bleeder current, through $R_{S1}$ and $R_{S2}$ (of Fig. 6.6) should be of the order of 2 mA and this current can be used to provide the required cathode voltage. Neglecting $I_S$ and $I_K$, and allowing for the cathode voltage,

$$\frac{R_{S2}}{R_{S1} + R_{S2}} = \frac{58\text{ V}}{248\text{ V}},$$

so $R_{S1} = 3R_{S2}$. Make $R_{S1} = 27\text{ k}\Omega$ and $R_{S2} = 82\text{ k}\Omega$. The bleeder current is then

$$I_B = \frac{V_{AA}}{R_{S1} + R_{S2}} = 2{\cdot}3\text{ mA}.$$

*Cathode resistor.* Neglecting $I_S$ and $I_K$,

$$R_K = \frac{V_K}{I_B} = \frac{2\text{ V}}{2{\cdot}3\text{ mA}} = 0{\cdot}9\text{ k}\Omega.$$

This may be made up of a fixed 680 Ω resistor in series with a 500 Ω variable resistor for zeroing purposes.

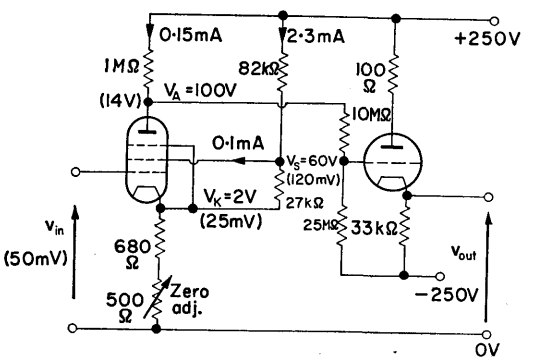



FIG. 6.11. Signal voltages (in brackets) and d.c. conditions shown in the circuit of Design Example 6.2. The large values of grid resistors for $V_2$ are permissible because of the high degree of negative feedback inherent in a cathode follower.

*Voltage divider.* To reduce loading on $R_L$, make $R_1 + R_2$ greater than $10R_L$.

$$\frac{R_1}{R_2} = \frac{V_A}{-V_{KK}} = \frac{100\text{ V}}{250\text{ V}} = \frac{10\text{ M}\Omega}{25\text{ M}\Omega}.$$

With these values the grid path resistance is considerably larger than the usual maximum of 3 MΩ, but as long as the grid current is of the order of $10^{-8}$ A this will generally cause no trouble. From previous considerations make $R_{K2} = 33\text{ k}\Omega$, as in Fig. 6.11.

*Estimation of gain.* Referring to Fig. 6.10 and using the expression,

$$\text{Voltage gain} = g_m \cdot \frac{R_L r_a}{R_L + r_a} \quad \text{where} \quad r_a \doteqdot 8\text{ M}\Omega,$$

$$g_m = \text{gain} \times \left(\frac{r_a + R_L}{R_L r_a}\right),$$

$$= 400 \times 1{\cdot}12 \times 10^{-6} \doteqdot 0{\cdot}45\text{ mA/V}.$$

Neglecting $r_a$, the presence of cathode resistance causes a reduction in the effective value of mutual conductance to $g'_m$ where

$$g'_m = \frac{g_m}{1 + g_m R_K} = \frac{0{\cdot}45}{1 + 0{\cdot}45}\text{ mA/V},$$

i.e. $$g'_m = 0{\cdot}31\text{ mA/V}.$$

The pentode gain, neglecting negative feedback due to finite screen resistance $= -g'_m R_L = 0{\cdot}31 \times 10^6 \times 10^{-3} = -310$. (The effective $r_a$ of the valve $= r_a + (\mu + 1)\, R_K = 8\text{ M}\Omega + 3\text{ M}\Omega$.)

The coupling resistors $R_1$ and $R_2$ reduce the gain by the factor

$$\frac{R_2}{R_1 + R_2} = \frac{25}{10 + 25}.$$

Thus, over-all gain

$$A = \frac{v_{out}}{v_{in}} = -310 \times 5/7 = -221.$$

*Frequency response.* An equivalent circuit of the amplifier is drawn in Fig. 6.12a, which may be reasonably simplified to the circuit of Fig. 6.12b.

Since $R_L' \ll R_1 + R_2$, a breakpoint occurs at $\omega_1 = 1/T_1 = 1/C_a R_L'$, and another at $\omega_2 = 1/T_2 = 1/C_{g2}R$, where $R = R_1 R_2/(R_1 + R_2)$. The approximate gain expression is

$$A(s) = \frac{g_m}{1 + g_m R_K} \cdot \frac{R_L'}{1 + sC_a' R_L'} \cdot \frac{R_2}{R_1 + R_2} \times \times \frac{1}{1 + sC_{g2} R_1 R_2/(R_1 + R_2)}. \tag{6.9}$$

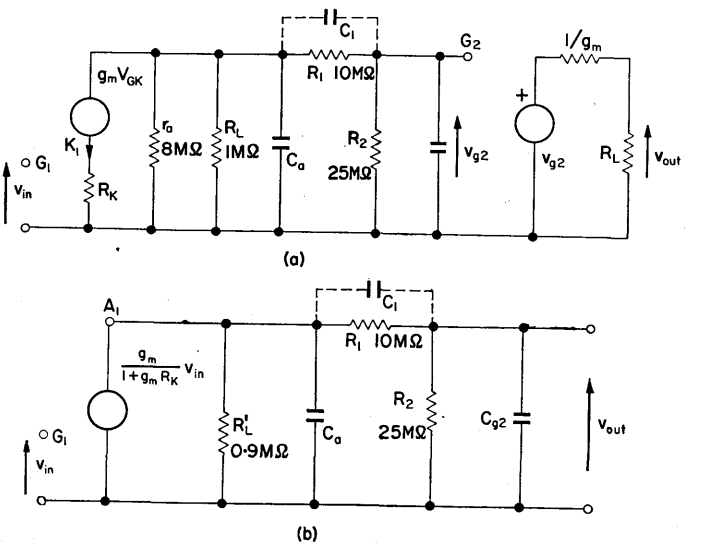



FIG. 6.12. Equivalent networks of the d.c. amplifier. The simplified network is valid because the gain of the cathode follower is unity and its bandwidth is much greater than that of the pentode stage. It can therefore be omitted for frequency considerations.

It is apparent that the capacitance across $R_2$, which is largely the input capacitance to the output stage, introduces a lag additional to that due to $C_a$. This additional lag can be eliminated by shunting $R_1$ with capacitance $C_1 = C_{g2}(R_2/R_1)$, i.e. the time constant $C_1R_1 = C_{g2}R_2$.

The gain expression is thus:

$$A(s) = g'_m \cdot \frac{R'_L}{1 + sC'_aR'_L} \cdot \frac{R_2}{R_1 + R_2} \times$$

$$\times \frac{1 + sC_1R_1}{1 + s(C_{g2} + C_1)\,[R_1R_2/(R_1 + R_2)]}$$

$$= g'_m \cdot \frac{R'_L}{1 + sC'_aR'_L} \cdot \frac{R_2}{R_1 + R_2}$$

(if $C_1R_1 = C_2R_2$).

$C_1$ has the effect of increasing $C_a$ by the term $C_1C_{g2}/(C_1 + C_{g2})$, i.e.

$$C'_a = C_a + \frac{C_1C_{g2}}{C_1 + C_{g2}},$$

and

$$\omega'_1 = \frac{1}{C'_aR'_L},$$

which is considerably less than $\omega_1$.

*Estimation of frequency response.* Referring to Fig. 6.12b,

$$C_a = C_{ak} + \text{socket and wiring capacitance} = 12\text{ pF}.$$

$$R'_L = r_aR_L/(r_a + R_L) = 0{\cdot}9\text{ M}\Omega.$$

Therefore

$$T_1 = C_aR'_L = 1{\cdot}08 \times 10^{-6}\text{ sec}.$$

$$\omega_1 = 2\pi f_1 = \frac{1}{C_aR'_L} = 92{\cdot}6 \times 10^3\text{ r/s},$$

from which

$$f_1 = 14{\cdot}75\text{ kc/s}.$$

$C_{g2} = C_{ga} + (1 - A)\,C_{gk}$ + wiring capacitance, where $A$ is the cathode follower gain. Since $A$ is very nearly unity, the input capacitance $C_{g2}$ is approximately equal to $C_{ga}$ + socket capacitance between the grid connection and earth. Thus,

$$C_{g2} \doteqdot 8\,\text{pF}.$$

$$\omega_2 = 2\pi f_2 = \frac{1}{C_{g2}R_1R_2/(R_1 + R_2)}$$

$$= \frac{1}{8 \times 10^{-12} \times 7{\cdot}1 \times 10^6} = 1{\cdot}76 \times 10^4\,\text{r/s}.$$

Therefore

$$f_2 = \omega_2/2\pi = 2{\cdot}8\,\text{kc/s}.$$

To remove the breakpoint at $f_2$, capacitor $C_1$ is used.

$$C_1R_1 = C_{g2}R_2.$$

Therefore

$$C_1 = C_{g2}\frac{R_2}{R_1} = 8 \times 25/10 = 20\,\text{pF}.$$

This increases the anode capacitance of $V_1$,

$$C_a' = C_a + \frac{C_1C_{g2}}{C_1 + C_{g2}} = 19\,\text{pF}.$$

Thus

$$\omega_1' = 2\pi f_1' = \frac{1}{C_a'R_L'} = 58{\cdot}5 \times 10^3\,\text{r/s},$$

and

$$f_1' = \omega_1'/2\pi = 9{\cdot}3\,\text{kc/s}.$$

The effect of $C_1$ on the amplitude response is illustrated in Fig. 6.13.

*Alternative coupling networks.* The reduction in gain due to the voltage divider can be eliminated by using a constant

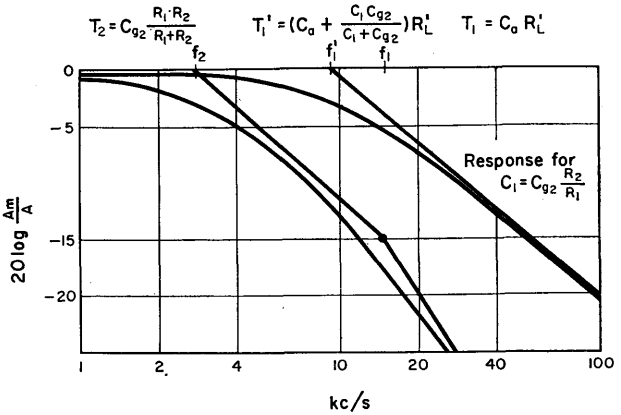



FIG. 6.13. Frequency response of the amplifier of Fig. 6.11. There are break points at $f_1$ due to the pentode and at $f_2$ because of the coupling network. The latter can be eliminated by introducing $C_1$ but this lowers $f_1$ to $f_1'$.

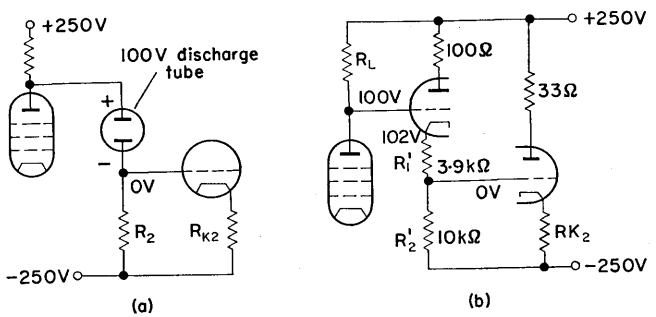



FIG. 6.14. Alternative coupling networks. (a) Use of gas discharge tube, and (b) cathode follower coupling. The former eliminates loss in gain due to resistive coupling. In the latter case the cathode follower isolates the anode voltage from the potential divider thus enabling low value resistors to be used. This gives improved stabilization of the operating point and effectively eliminates the breakpoint $f_2$ due to the coupling network.

voltage device, such as a discharge tube. The disadvantages of this method are chiefly:

(a) A relatively large current is required to operate the device in its constant voltage region, and this current produces a voltage across $R_L$ reducing the available anode swing.

(b) Unless the gas tube is of a special type, it is likely to produce noise voltage and even oscillate. Special devices have been produced which, at least partially, overcome these defects.

The large value of resistors $R_1$ and $R_2$ in Fig. 6.6 can be reduced by isolating the pentode anode from the potential divider with a cathode follower as shown in Fig. 6.14b.

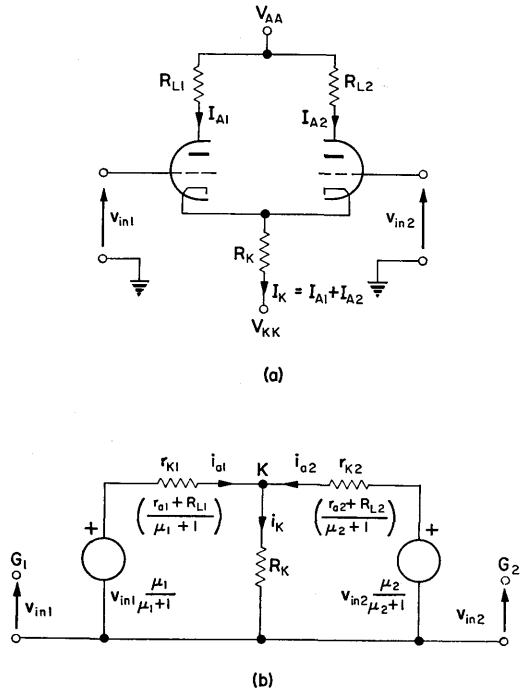



FIG. 6.15. Cathode coupled amplifier with equivalent network.

## 6.4. The Cathode Coupled Amplifier

A circuit which is used to reduce drift in direct coupled amplifiers is the balanced cathode coupled amplifier or longtail pair shown in Fig. 6.15a. When $v_{in1} = 0$, for two identical valves, the standing currents

Also,

$$I_{A1} + I_{A2} = I_K, \quad \text{and} \quad I_{A1} = I_{A2} = \frac{I_K}{2}.$$

$$I_K = \frac{V_{RK}}{R_K} \doteqdot \frac{-V_{KK}}{R_K}$$

(where $V_{KK} \gg V_{GK}$, and $V_{RK}$ is the voltage across the cathode resistor).

*Small Signal Representation*

The small signal performance can be assessed by analysing the equivalent network.

A simpler approach can be made by regarding the amplifier as two cathode followers with common cathode resistor, having the equivalent network of Fig. 6.15b.

The incremental anode current, $i_{a1}$ and $i_{a2}$, may be found by circuital analysis. (See Appendix A.)

$$(r_{k1} + R_K)\, i_1 - R_K i_2 = \frac{\mu_1}{\mu_1 + 1} \cdot v_{in1}, \tag{6.10}$$

$$-R_K i_1 + (R_K + r_{k2})\, i_2 = \frac{-\mu_2}{\mu_2 + 1} \cdot v_{in2}. \tag{6.11}$$

Thus,

$$i_1 = i_{a1}$$

$$= \frac{(R_K + r_{k2})\,[1/(\mu_1 + 1)]\, v_{in1} - [1/(\mu_2 + 1)]\, R_K \cdot v_{in2}}{r_{k1} \cdot r_{k2} + R_K(r_{k1} + r_{k2})},$$

$$i_2 = i_{a2}$$

$$= \frac{[\mu_1/(\mu_1 + 1)]\, R_K \cdot v_{in1} - (R_K + r_{k1})\,[\mu_2/(\mu_2 + 1)]\, v_{in2}}{r_{k1} \cdot r_{k2} + R_K(r_{k1} + r_{k2})}.$$

It is apparent from Fig. 6.15b (and the above equations) that if $R_K \gg r_{k1}$ and $r_{k2}$,

$i_{a1} \doteqdot -i_{a2}$ (as the signal current in $R_K$ will be negligible).

Thus

$$i_{a1} = \frac{[\mu_1/(\mu_1 + 1)]\, v_{in1} - [\mu_2/(\mu_2 + 1)]\, v_{in2}}{r_{k1} + r_{k2}}.$$

Therefore

$$v_{a1} = -i_{a1} R_{L1}$$

$$= \frac{[-\mu_1/(\mu_1 + 1)]\, v_{in1} + [\mu_2/(\mu_2 + 1)]\, v_{in2}}{r_{k1} + r_{k2}} \cdot R_{L1},$$

and

$$v_{a2} = \frac{[\mu_1/(\mu_1 + 1)]\, v_{in1} - [\mu_2/(\mu_2 + 1)]\, v_{in2}}{r_{k1} + r_{k2}} \cdot R_{L2}.$$

If

$$\mu_1 = \mu_2 = \mu,\ r_{a1} = r_{a2} = r_a \quad \text{and} \quad R_{L1} = R_{L2} = R_L,$$

$$v_{a1} = -v_{a2} = \frac{-\mu R_L (v_{in1} - v_{in2})}{2(r_a + R_L)}. \tag{6.12}$$

For

$$v_{in2} = 0, \quad \frac{v_{a1}}{v_{in}} = \frac{-\mu R_L}{2(r_a + R_L)}. \tag{6.13}$$

i.e. half the gain of a common cathode amplifier, and

$$\frac{v_{a2}}{v_{in}} = \frac{+\mu R_L}{2(r_a + R_L)}. \tag{6.14}$$

If

$v_{in1} = v_{in2}$ there will be no output.

For a differential input,

$$v_{in1} = -v_{in2}, \quad \frac{v_{a1}}{v_{in}} = \frac{-\mu R_L}{r_a + R_L}. \tag{6.15}$$

These relationships are shown in Fig. 6.16a.

For a differential output taken across the two anodes, the gain is $-\mu R_L/(r_a + R_L)$ for a single input.

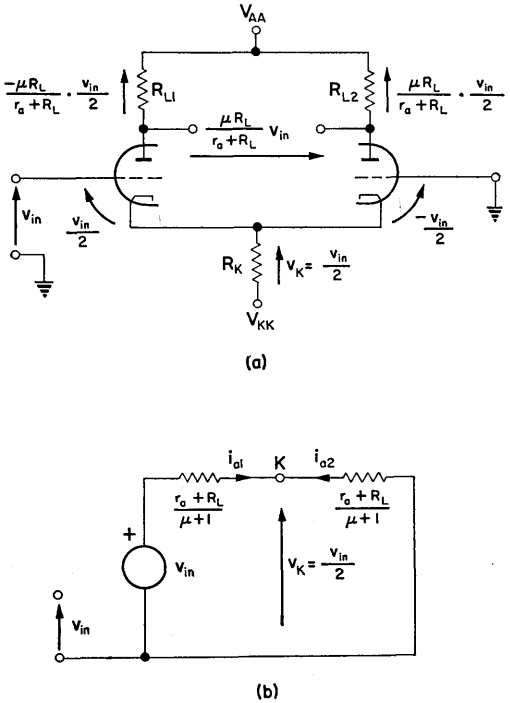



FIG. 6.16. (a) Distribution of signal voltages in cathode coupled amplifier. (b) The equivalent network is obtained for identical valves and a large value of $R_K$, with the input voltage at grid 1 and the second grid earthed.

*Common Mode*

If identical signals are applied to the two inputs of a longtail pair, any output voltage produced is the common mode output. Because of its symmetrical nature, when common mode signals are applied, the network can be considered as having one valve

made up of the two valves in parallel. Thus, from Fig. 6.17,

Common mode gain

$$= \frac{-v_a}{v_{in}} = \frac{-\mu R_L}{(r_a/2) + (R_L/2) + (\mu + 1)\,R_K} = A_{cm}. \tag{6.16}$$

For large $\mu$ and where $\mu R_K$ is very much larger than $r_a$ and $R_L$,

$$A_{cm} \doteqdot -R_L/2R_K.$$

If $R_K$ is very large the approximation of Fig. 6.16b is valid and the common mode gain is zero.

In direct coupled amplifiers it is desirable to have a low common mode gain as the drift sources are largely common mode. A change in heater current affects both valves in the same manner, and if the common mode gain is low the output voltage developed as a result of this change will be small. For a single valve the drift voltage would be amplified by the full gain.

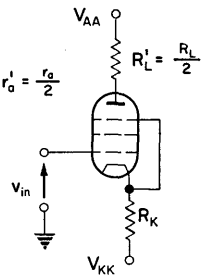



FIG. 6.17. Cathode coupled amplifier represented by a single valve for the determination of common mode effects.

*Difference Amplifier*

From eqn. (6.12) it is apparent that the longtail pair can be used as a difference amplifier:

$$v_{a1} = -v_{a2} = \frac{-\mu(v_{in1} - v_{in2})}{2(r_a + R_L)} \cdot R_L.$$

For this to be true the common mode gain must be very small.

*Constant Current Tail.*

From Fig. 6.15b, $i_{a1} + i_{a2} = i_k$. If $i_k$ is held constant, the common mode gain is zero since the anode currents cannot increase. $R_K$ cannot be increased since, for a given supply voltage,

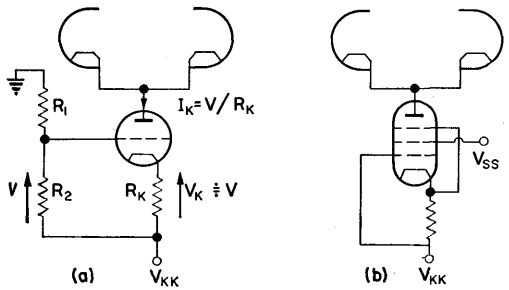



FIG. 6.18. The use of (a) a cathode follower and (b) a pentode, to provide constant cathode current. By this means the common mode gain is very much reduced.

it determines the standing currents. Devices that simulate a large resistance, largely independent of the standing current, are known as constant current devices.

(a) *Cathode follower.* By cathode follower action the voltage across $R_K$ is maintained constant with anode voltage changes.

EXAMPLE. Referring to Fig. 6.18a, if $V_{KK} = -300$ V and a constant current of 5 mA is required, let $V$ be 100 V. Suitable values of $R_1$ and $R_2$ are 680 kΩ and 330 kΩ respectively and $R_K = 100$ V/5 mA = 20 kΩ. From the characteristics of an ECC81, $V_A = 200$ V, $I_A = 5$ mA, and $V_{GK} = -2{\cdot}2$ V.

(b) *Pentode.* From typical pentode characteristics it is apparent that, for a constant grid voltage, a pentode will pass constant current over a large range of anode voltage. The use of a pentode to serve this function is illustrated in Fig. 6.18b.

*Design of Cathode Coupled Amplifiers*

Because of the negative feedback inherent in the circuit, the design procedure is relatively straight forward.

DESIGN EXAMPLE 6.3 (Fig. 6.19)

Required, a cathode coupled amplifier using an ECC81 double triode, the standing anode voltage to be 100 V at each anode. The voltage supplies available are: $V_{AA} = 250$ V and $V_{KK} = -250$ V.

The operating conditions can be found independently of the valve, provided that it can supply the required current. The

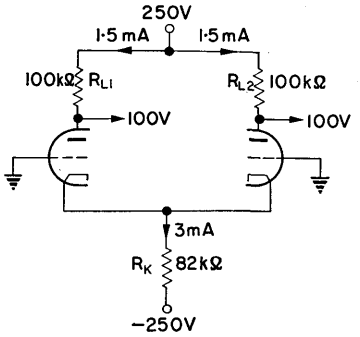



FIG. 6.19. Circuit arrangement of the symmetrical cathode coupled amplifier (or longtail pair) of Design Example 6.3.

cathode current is determined by $R_K$ since the cathode is at approximately 0 V.

Let the two anode loads, $R_L$, be 100 kΩ.

$$I_{A1} = I_{A2} = (V_{AA} - V_A)/R_L = 150 \text{ V}/100 \text{ k}\Omega = 1{\cdot}5 \text{ mA}.$$

$$I_K = I_{A1} + I_{A2} = 2 \times 1{\cdot}5 \text{ mA} = 3 \text{ mA}.$$

$$R_K = V_{KK}/I_K = 250 \text{ V}/3 \text{ mA} = 83{\cdot}3 \text{ k}\Omega.$$

Let it be 82 kΩ which is a preferred value.

*Gain at anode 2.* From the valve data, $\mu = 60$ and $r_a = 20$ kΩ. Using eqn. (6.14),

$$A = \frac{\mu R_L}{2(r_a + R_L)} = \frac{60 \times 100\ \text{k}\Omega}{2(20\ \text{k}\Omega + 100\ \text{k}\Omega)} = 25.$$

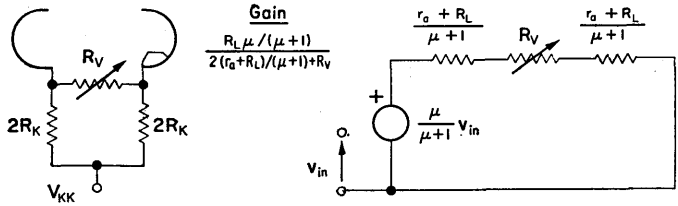



FIG. 6.20. Gain control for longtail pair with its equivalent circuit.

The cathode circuit of Fig. 6.20 enables the gain of the amplifier to be controlled, by reducing the coupling between the two halves.

*Frequency response of the longtail pair.* An equivalent circuit may be drawn to show that the amplifier of Fig. 6.14 has a single lag. This is done in Fig. 6.21.

$$\omega_1 = \frac{1}{C_s R}, \quad \text{where} \quad R = \frac{R_L[r_a + (\mu + 1)\, r_k']}{R_L + r_a + (\mu + 1)\, r_k'} \tag{6.17}$$

and

$$r_k = \frac{r_a + R_L}{(\mu + 1)}, \quad r_k' = \frac{R_K r_k}{R_K + r_k}.$$

Substituting values,

$$R = 58\ \text{k}\Omega \quad \text{and} \quad C_s = 3\ \text{pF}.$$

Thus,

$$T_1 = 0{\cdot}174 \times 10^{-6}\ \text{sec},$$

$$\omega_1 = 5{\cdot}75 \times 10^6\ \text{r/s}, \quad \text{and} \quad f_1 = 920\ \text{kc/s}.$$

A convenient way of measuring the shunt capacitance $C_s$ is to find $f_1$, that is the 3 dB point, and then add shunt capacitance until the 3 dB point is at $\frac{1}{2}f_1$. The added capacitance is

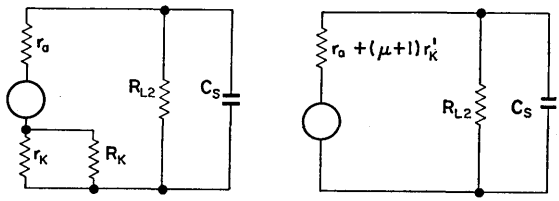



FIG. 6.21. Equivalent network of longtail pair for the evaluation of frequency response.

then equal to the actual shunt capacitance $C_s$ together with the capacitance of the measuring probe.

*Coupling network.* If the longtail pair is to be used as a low drift input stage to the pentode–cathode follower amplifier it must be direct coupled to the pentode stage.

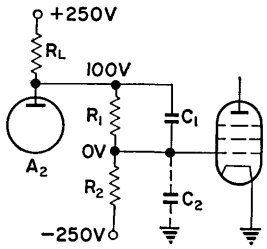



FIG. 6.22. Coupling between longtail pair and pentode stage.

Let the design value for $V_{A2}$ be 100 V as in Fig. 6.22. $R_1 + R_2$ is made much greater than $R_L$ so that the gain is not reduced by loading:

$$\frac{R_1}{R_2} = \frac{100\text{ V}}{250\text{ V}} = \frac{1\text{ M}\Omega}{2{\cdot}5\text{ M}\Omega}.$$

To elimimate the time constant due to $C_2$, make $C_1R_1 = C_2R_2$.

A method of finding a value for $C_1$ is to inject a rectangular waveform at the anode and adjust $C_1$ to give a flat top to the waveform at the grid, when displayed on an oscilloscope, as shown in Fig. 6.23.

EXAMPLE. The measured $C_1 = 150\,\text{pF}$, and from consideration of the time constants,

$$C_2' = 60\,\text{pF}.$$

But

$$C_2 = C_2' - C_{\text{probe}}$$

$$= 49\,\text{pF for a probe capacitance of } 11\,\text{pF}.$$

Therefore

$$C_1 = \frac{C_2 R_2}{R_1} = 120\,\text{pF} \quad \text{(in the absence of the probe)}.$$

$C_1$ and $C_2$ in series, increase the shunt capacitance by 35 pF, making it 38 pF. (See Fig. 6.24.)

$$\omega_1 = \frac{1}{C_s R} = \frac{10^9}{38 \times 56} = 4{\cdot}7 \times 10^5\,\text{r/s}.$$

$$T_1 = C_s R = 2{\cdot}13 \times 10^{-6}\,\text{sec}.$$

$$f_1 = \omega_1/2\pi \doteqdot 75\,\text{kc/s}.$$

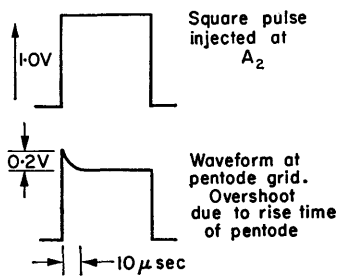



FIG. 6.23. For a square wave input injected at $A_2$, $C_1$ is adjusted until the flat top of the lower waveform is obtained. The peak is due to Miller effect at the grid of the pentode.

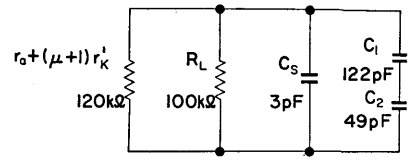



FIG. 6.24. Increase in effective shunt capacitance by the coupling network.

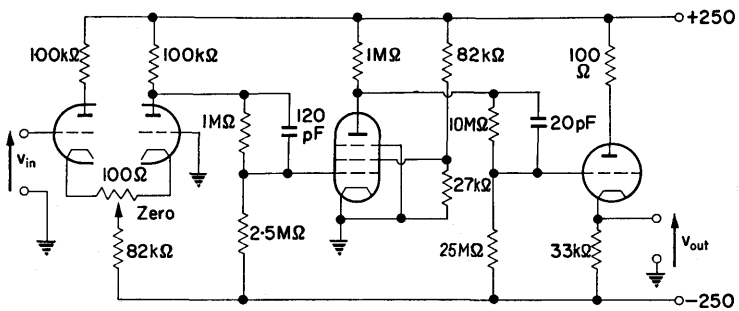



FIG. 6.25. The final circuit of a three-stage d.c. amplifier.

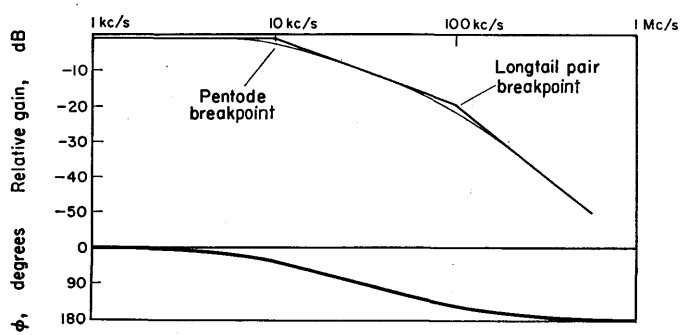



FIG. 6.26. Frequency response of the three-stage amplifier.

Gain from the grid of the longtail pair to the grid of the pentode $= 25 \times 5/7 = 18$. The completed circuit of a three-stage amplifier, consisting of a longtail pair input, pentode amplifier and cathode follower output is given in Fig. 6.25. Its frequency response is shown in Fig. 6.26.

## 6.5. Direct Coupled Transistor Amplifiers

Most transistors can be operated with very low collector voltages, of the same order as the voltage required to bias the base of a following stage. Referring to Fig. 6.27, if $V_{CC}$ is much

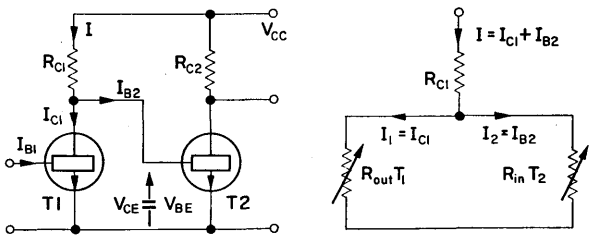



FIG. 6.27. Direct coupled transistor amplifier with network to represent the division of current between the collector of $T_1$ and the base of $T_2$.

greater than $V_{CE}$, then the current $I = (V_{CC} - V_{CE})/R_C$ will be relatively constant. When $T_1$ is bottomed $V_{BE}$ is very small and $T_2$ will be non-conducting.

As the base current of $T_1$ is reduced, $V_{BE}$ rises and $T_2$ starts to conduct and as $I_1$ decreases, $I_2$ increases, until when $T_1$ is non-conducting, $I_2 = I$. The amplifier action may therefore be considered as the exchange of $I$ between $I_1$ and $I_2$ due to the variations in $T_1$ output resistance $R_{out}$, and $R_{in}$, the input resistance of $T_2$. $R_{in}$ is the forward biased diode resistance of the base emitter junction and, due to its characteristic, the voltage $V_{BE}$ across it is limited. Since $R_C$ is made much greater than $R_{in}$, $R_{in}$ is effectively the load resistance of $T_1$.

EXAMPLE. Let $R_{C1} = 15\,\text{k}\Omega$, $R_{C2} = 3{\cdot}9\,\text{k}\Omega$, $V_{CC} = 6\,\text{V}$ and $I = 0{\cdot}4\,\text{mA}$. The load line may be constructed, as in Fig. 6.28a, in the following manner. The input characteristic $OAB$ of $T_2$ is superimposed on the collector characteristic of $T_1$, and then

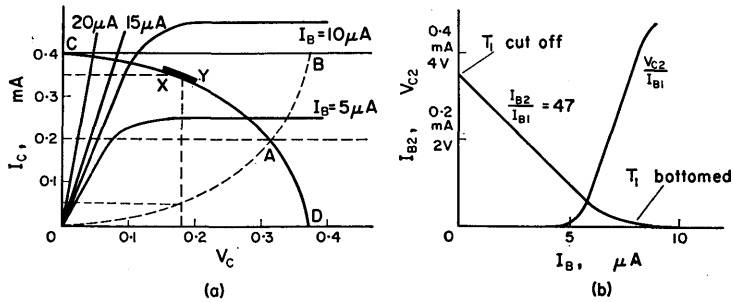



FIG. 6.28. (a) The load line of $T_1$, of Fig. 6.27, is the curve $CD$ of which the section $XY$ is the region of operation. From this load line the current gain for the first stage can be derived. Also shown (b) is the transfer characteristic $V_{C2}/I_{B1}$.

rotated about the axis drawn at $I_C = I/2$ (in this case 0·2 mA), giving the curve $CAD$. The line $CB$ represents the constant current $I = 0{\cdot}4\,\text{mA}$.

For any voltage $V_C$, a vertical line joining the voltage axis to the line $CB$ is divided into two parts such that the part of the vertical above the curve $CAD$ represents the current $I_{B2}$, the part below being $I_{C1}$. Thus, at $V_C = 0{\cdot}18\,\text{V}$, $I_{C1} = 0{\cdot}35\,\text{mA}$ and $I_{B2} = 0{\cdot}05\,\text{mA}$.

It is apparent that the operating part of the load line must be near the bottomed end of the curve, since $T_2$ requires a base current that is very much less than $I(= 0{\cdot}4\,\text{mA})$. In Fig. 6.28a the operating part is indicated by the line $XY$, and as the voltage $V_{C1}$ changes by only a small amount $R_{in}$ (the slope of $XY$) remains relatively constant. Generally, $R_{in}$ will be much less than $R_{C1}$ and efficient current transfer can be effected. At low values of $I_{B2}$ the transfer resistance decreases as is indicated by the slope of the $V_{C2}/I_{B1}$ curve of Fig. 6.28b, thus introducing a degree of

non-linearity. Where $T_2$ is required to provide a voltage output, this has the effect of limiting the effective output voltage swing.

The linearity of the stage can be improved by biasing the emitter and thus moving the load line to the right. Methods of

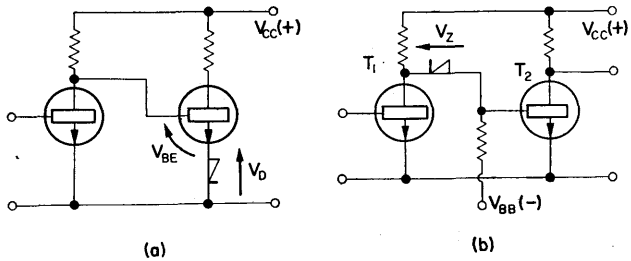



FIG. 6.29. A forward biased diode (a) provides emitter bias which has the effect of shifting the load line of Fig. 6.28 to the right, thus improving linearity. A similar effect is obtained in (b) by the use of a Zener diode.

obtaining such bias are given in Chapter 2. Alternatively, as shown in Fig. 6.29a, a forward biased junction diode will provide a constant voltage of approximately 0·2 V which is usually adequate.

Figure 6.29b shows how a Zener diode may be used to provide a low resistance voltage drop which does not unduly increase $R_{IN}$ for $T_2$. It may be replaced by a resistor through which a constant current is drawn.

An approximate small signal equivalent network is shown in Fig. 6.30.

*Complementary Devices*

With a *pnp* device, it is possible to use an *npn* as the next stage as in Fig. 6.31. This arrangement is particularly advantageous when the required output is about zero volts.

$T_2$ will be cut off when $T_1$ is cut off. Care must be taken to ensure that the leakage current of $T_1$ does not produce so large a voltage across $R_{C1}$ that $T_2$ is permanently bottomed. If $V_{BE2}$

is of the order of 200 mV, $R_{in}$ for $T_2$ will be low, and if $R_{C1}$ is much greater than $R_{in}$ the leakage current $I_{CEO}$ will flow into the base of $T_2$. If $T_1$ has a large leakage current either $R_{C1}$ must be kept small or a base resistor for $T_2$ should be used. Both these methods reduce the current gain.

DESIGN EXAMPLE 6.4

Required, a d.c. amplifier with voltage gain greater than 5000 and providing signal inversion. The output resistance should be less than 1 kΩ and the output voltage swing ±5 V.

The circuit diagram will take the form shown in Fig. 6.32.

*Supply voltages.* The output voltage is required to be ±5 V. Let the supply voltage be ±8 V. The output transistor must have $V_{CE(max)}$ greater than 16 V.

*Transistors.* OC44 transistors are suitable for direct coupling. The minimum current gain of two OC44 transistors, $A_1 = 30 \times 30 = 900$.

As overall signal inversion is required, an odd number of common emitter stages is necessary, and an *npn* transistor with adequate collector voltage and power rating is required for the output stage. An OC139 would be suitable as it has a 20 V collector rating, 100 mV dissipation at 25 °C and current gain greater than 20.

*Output load resistor* $R_{C3}$. A 1 kΩ resistor will ensure that the output resistance is less than 1 kΩ. With this load resistor the current gain $A_2 \doteqdot 20$.

$$P_{C(max)} = 8 \text{ V} \times 8 \text{ mA} = 64 \text{ mW}.$$

*Gain.* Voltage gain

$$A_v = A_i \cdot \frac{R_L}{R_{in}},$$

where

$$A_i = A_1 A_2 \doteqdot 900 \times 20 = 18 \times 10^3.$$

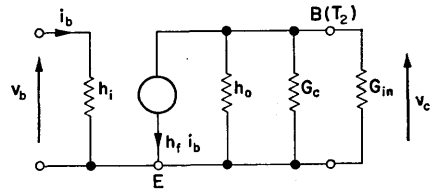



FIG. 6.30. Approximate small signal equivalent network for the evaluation of performance of a direct coupled transistor stage. Normally, $G_{in}$ is much greater than $h_o$ and $G_C$ which may therefore be neglected.

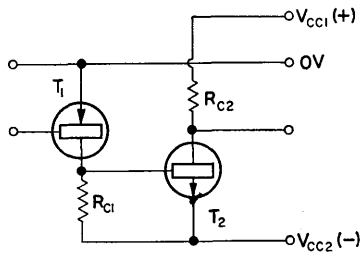



FIG. 6.31. Use of a complementary pair of transistors to provide an output voltage varying about zero.

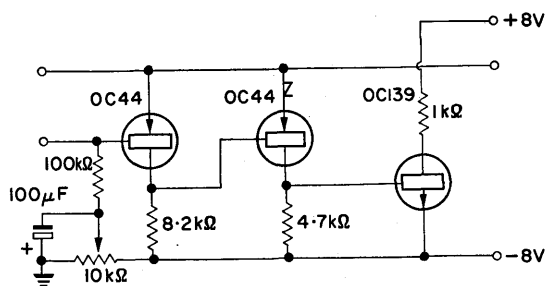



FIG. 6.32. Circuit diagram of Design Example 6.4. The 10 kΩ potentiometer enables the output voltage to be set to zero.

If $R_L = 1\,\text{k}\Omega$ and $R_{\text{in}} = 2\,\text{k}\Omega$ (approximately equal to $h_i$), then $A_V = -9000$.

This figure ensures that a higher value of $R_{\text{in}}$, or reasonable loading of $R_{C3}$ by an external load, will not cause the gain to fall below the specified value.

*$R_{C1}$ and $R_{C2}$.* A suitable current for the direct coupled pair is 1 mA.

$$R_{C1} \doteqdot \frac{V_{CC}}{I_C} = 8{\cdot}2\,\text{k}\Omega \quad \text{(a preferred value)}.$$

As $R_{C2}$ is a compromise between the current transfer and the voltage produced by leakage current, $4{\cdot}7\,\text{k}\Omega$ is a suitable value.

*Biasing of $T_2$.* To improve linearity, the emitter of $T_2$ is held at $-0{\cdot}6$ V by a forward biased silicon diode, as shown in Fig. 6.29a.

*Zero control.* A base current control is required for $T_1$, to enable the output voltage to be set to zero.

## 6.6. Drift in Transistor D.C. Amplifiers

The input-referred current drift can be expressed as:

$$I_{di} = \Delta I_{CBO} + \frac{\Delta V_{BE}}{R_S} + I_B \cdot \frac{\Delta h_F}{h_F} \qquad (6.18)$$

$$= \underset{\text{(a)}}{\text{leakage current}} + \underset{\text{(b)}}{\text{change in } V_{BE} \text{ required to maintain constant } I_C} + \underset{\text{(c)}}{\text{change in } h_F}$$

(a) The leakage current is a function of temperature. Use of silicon transistors greatly reduces $I_{CBO}$.

(b) As the temperature is increased, a decrease in $V_{BE}$ is required to maintain a constant collector current. A change of 2–4 mV per °C is commonly quoted.

It is apparent that increasing the source resistance decreases the effect of $\Delta V_{BE}$ which becomes zero for a current fed transistor. If the amplifier has to operate from a low resistance source, $\Delta V_{BE}$ can be balanced out by using a compensating system. Often the most satisfactory method is a longtail pair or symmetrical emitter coupled system.

Both transistors should be kept at the same temperature, otherwise, even for identical units, drift would result.

*Longtail Pair Analysis*

The equivalent network is simplified by considering $R_{C1} = R_{C2} = R_C$. Assume identical transistors, $h_{re} = 0$ and $h_{oe} \ll 1/R_C$ as in Fig. 6.33b.

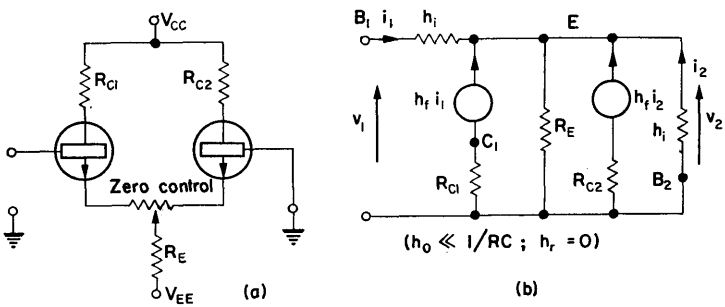



FIG. 6.33. Transistor longtail pair with equivalent network.

Writing the equations for the nodes $B_1$ and $E$,

$$\frac{1}{h_i} \cdot v_1 - \frac{1}{h_i} \cdot v_2 = i_1, \tag{6.19}$$

$$-\frac{1}{h_i} v_1 + v_2 \left[\frac{2}{h_i} + \frac{1}{R_E}\right] = h_f i_1 + h_f i_2. \tag{6.20}$$

From eqn. (6.19),

$$i_1 = \frac{v_1 - v_2}{h_i} \quad \text{and} \quad i_2 = \frac{-v_2}{h_i},$$

and, substituting in eqn. (6.20),

$$-\frac{1}{h_i}(1 + h_f)\, v_1 + \frac{1}{h_i}\left(2 + 2h_f + \frac{h_i}{R_E}\right) v_2 = 0.$$

Thus,

$$v_2 = \frac{1 + h_f}{2(1 + h_f) + (h_i/R_E)} \cdot v_1 \qquad (6.21)$$

$$\doteqdot \tfrac{1}{2} v_1 \quad \text{as} \quad h_i/R_E \ll 2(1 + h_f).$$

The input current,

$$i_1 = \frac{v_1}{2h_i},$$

and

$$r_{\text{in}} = \frac{v_1}{i_1} = 2h_i.$$

The output voltage at $C_1$,

$$v_{C1} = -h_f R_C i_1 = -\frac{h_f}{2h_i} R_C v_1$$

$$= \frac{-g_m R_C}{2} v_1. \qquad (6.22)$$

The $T_2$ base current,

$$i_2 = -\frac{v_2}{h_i} = -\frac{v_1}{2h_i}.$$

The output voltage at $C_2$,

$$v_{C2} = h_f R_C i_2 = \frac{h_f}{2h_i} R_C v_1$$

$$= \frac{-g_m R_C}{2} v_1. \qquad (6.23)$$

Note that half the input voltage $v_1$ is across the input transistor and half across the emitter resistor $R_E$.

DESIGN EXAMPLE 6.5

Required, a longtail pair to provide a voltage gain greater than 40, using supply voltages of $\pm 5$ V.

*Transistors.* Let the transistors be OC44 types with a $g_m$ greater than 30 mA/V.

*Collector resistor* $R_C$.

$$A_v = 40 = \frac{g_m R_C}{2} \quad \text{[from eqn. (6.23)]}.$$

Thus,

$$R_C = \frac{2A_v}{g_m} = \frac{2 \times 40}{30 \times 10^{-3}} = 2{\cdot}7\ \text{k}\Omega.$$

Let the standing voltage of the collectors for zero input be $-2{\cdot}5$ V. This allows a collector swing of $\pm 2{\cdot}5$ V about the quiescent value:

$$I_C = \frac{V_C - V_{CC}}{R_C} = \frac{2{\cdot}5\ \text{V}}{2{\cdot}7\ \text{k}\Omega} \doteqdot 1\ \text{mA}.$$

*Emitter resistor* $R_E$.

$$R_E \doteqdot \frac{V_{EE}}{2I_C} = \frac{5\ \text{V}}{2\ \text{mA}}.$$

Let it be 2·7 kΩ which is a preferred value.

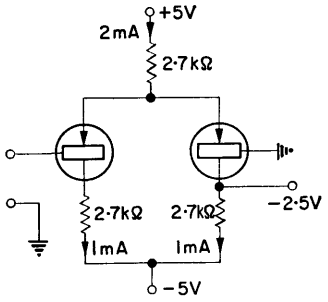



FIG. 6.34. Circuit diagram of Design Example 6.5.

*Dissipation* $P_{C(max)}$. 2·5 V × 1 mA = 2·5 mW which is well within the transistor rating.

The final circuit details are as shown in Fig. 6.34.

A knowledge of feedback theory is necessary to permit the further study of transistor zero frequency amplifiers. This is dealt with in Chapter 7.

CHAPTER 7

# Negative Feedback Amplifiers

## 7.1. Introduction

By feeding back a portion of the output to the input, the performance of an amplifier can be greatly changed. Figure 7.1 represents the flow of information in a feedback network. $A$ can be a voltage or current amplifier.

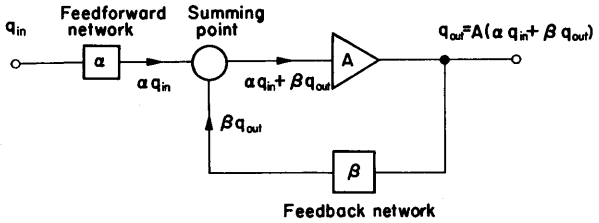



FIG. 7.1. Basic feedback structure. The input and output quantities, $q_{in}$ and $q_{out}$, can be either voltages or currents depending on the type of amplifier. $\alpha$ and $\beta$ are fractions of input and output signals appearing at the summing point.

### *Gain of Feedback Amplifier*

As shown in Fig. 7.1, the output quantity

$$q_{out} = A(\alpha q_{in} + \beta q_{out}) \tag{7.1}$$

or

$$q_{out} = \frac{\alpha A}{1 - A\beta} q_{in}. \tag{7.2}$$

In most examples $\alpha$ and $\beta$ will be made up of passive elements and have values of unity or less. The amplifier gain $A$ will generally be much greater than unity.

*Loop Gain*

The product $A\beta$ is the loop gain. It is usually much greater than unity and has a negative sign if the feedback is to be negative. Either $A$ or $\beta$ can be negative. If $A$ is negative the feedback amplifier will provide signal inversion.

For

$$-A\beta \gg 1,$$

$$q_{out} \doteqdot \frac{\alpha}{\beta} q_{in} \quad \text{[from eqn. (7.2)]}. \tag{7.3}$$

EXAMPLE. If $\alpha = 1$, $\beta = 0{\cdot}2$ and $A = -50$, the loop gain is $A\beta = -10$, and

$$q_{out} = \frac{-50}{1 + 10} q_{in} \quad \text{[from eqn. (7.2)]}$$

$$= -4{\cdot}5.$$

If the approximation of eqn. (7.3) is used

$$q_{out} \doteqdot \frac{1}{0{\cdot}2} q_{in} = -5.$$

If there is no signal inversion in the amplifier, that is $A = 50$, $\beta$ must be negative for negative feedback.

Then

$$q_{out} = \frac{50}{1 + 10} q_{in} \quad \text{[from eqn.(7.2)]},$$

and the output signal is of the same sign as the input signal.

*Stabilization of Gain*

Equation (7.3) shows that if the loop gain is sufficiently large the over-all gain is independent of the $A$ gain.

Let

$$\frac{q_{out}}{q_{in}} = G = \frac{\alpha A}{1 - A\beta},$$

then

$$\frac{dG}{dA} = \frac{(1 - A\beta) + A\beta}{(1 - A\beta)^2} \cdot \alpha = \frac{\alpha A}{1 - A\beta} \cdot \frac{1}{1 - A\beta} \cdot \frac{1}{A}$$

$$= \frac{G}{A(1 - A\beta)}.$$

Thus

$$\frac{\Delta G}{G} = \frac{\Delta A}{A} \cdot \frac{1}{1 - A\beta}, \tag{7.4}$$

where $(1 - A\beta) > 1$ for negative feedback, and $\Delta A/A$ and $\Delta G/G$ are fractional changes in $A$ amplifier gain and feedback amplifier gain respectively.

The change in $A$ gain is reduced by the term $1/(1 - A\beta)$ for the feedback amplifier. Since, in general, non-linear distortion arises from changes in gain with signal amplitude, such distortion is reduced by the same factor, when negative feedback is applied.

*Extension of Bandwidth*

The expressions of the previous paragraph show that changes in gain due to variation in frequency are reduced by the factor $1/(1 - A\beta)$. Thus the bandwidth of the $A$ amplifier is extended by this factor, as $1 - A\beta$ is greater than unity for negative feedback.

*Application of Negative Feedback*

Basic feedback connections are illustrated in Fig. 7.2.

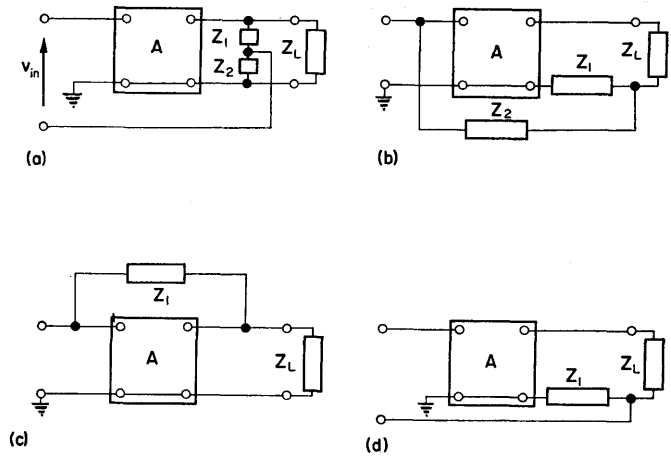



FIG. 7.2. Application of negative feedback. Voltage feedback is eliminated by short circuiting the output terminals. Current feedback is eliminated by open circuiting the output.

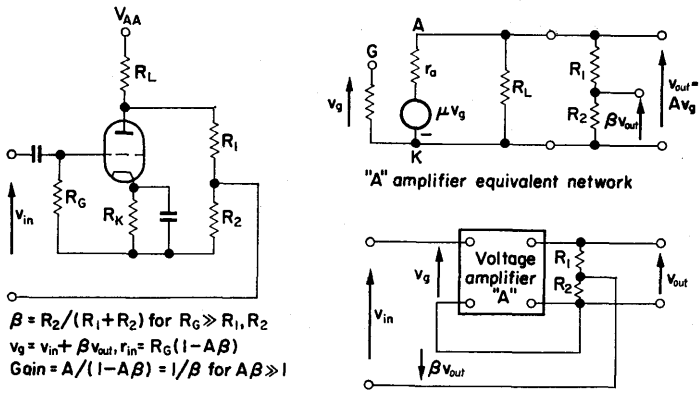



FIG. 7.3. Shunt–series feedback amplifier.

## 7.2. Examples of Negative Feedback Amplifiers

### (a) *Voltage Amplifier*

A voltage amplifier with a fraction of the output voltage fed back in series with the input voltage is characterized by high input impedance and low output impedance together with a defined voltage gain. (See Fig. 7.3.)

*Input impedance.*

$$z_{in} = \frac{v_{in}}{i_{in}}.$$

$$i_{in} = \frac{v_g}{z_g} = \frac{v_{in} + \beta v_{out}}{z_g} \quad \text{(where } z_g \text{ is the input impedance of the } A \text{ amplifier)}$$

$$= \frac{v_{in} + [A\beta v_{in}/(1 - A\beta)]}{z_g} \quad \left(\text{substituting } v_{out} = \frac{A}{1 - A\beta} v_{in}\right)$$

$$= \frac{[v_{in}/(1 - A\beta)]}{z_g},$$

or

$$z_{in} = (1 - A\beta)\, z_g. \tag{7.5}$$

The input impedance of the $A$ amplifier is increased by the factor $(1 - A\beta)$ for series input.

In general, when the feedback signal is applied in series with the input signal the input impedance is increased.

*Output impedance.*

$$z_{out} = \frac{v_{out}}{i_{out}}.$$

To determine the output impedance let $v_{in}$ be zero, then without feedback ($\beta = 0$), the output impedance is $z_{oA}$ which is $R_L$ and $(R_1 + R_2)$ in parallel.

Referring to Fig. 7.4, let an alternating voltage $v_{out}$ be placed across the output terminals. Then, if $\beta$ is not zero,

$$i_{out} = \frac{v_{out} - A\beta v_{out}}{z_{oA}},$$

or

$$z_{out} = \frac{z_{oA}}{1 - A\beta}. \tag{7.6}$$

The output resistance of the $A$ amplifier is reduced by the factor $1/(1 - A\beta)$.

In general, when the feedback signal is derived from a parallel network the output impedance is decreased by negative feed-

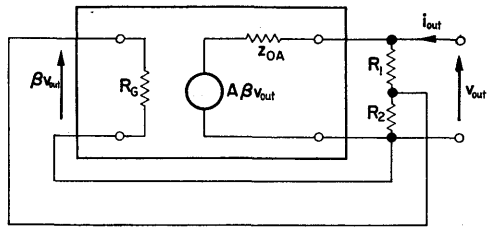



FIG. 7.4. Measurement of output impedance.

back. The test for parallel (or voltage) feedback is to disconnect the load and observe that the feedback loop is still operative.

*Cathode follower.* This is an example of a shunt–series amplifier, and is shown in Fig. 7.5.

The gain,

$$A = \frac{v_{out}}{v_{gk}} = \frac{\mu R_K}{r_a + R_K}.$$

There is no signal inversion as the output signal is obtained from between the cathode and common terminal.

The output is fed back in series with the input signal without attenuation. Thus, $\beta = -1$ and $\alpha = 1$.

$$G = \frac{\alpha A}{1 - A\beta} \quad \text{[from eqn. (7.2)]}$$

$$= \frac{[\mu R_K/(r_a + R_K)]}{1 + [\mu R_K/(r_a + R_K)]}$$

$$= \frac{\mu R_K}{r_a + R_K(\mu + 1)}$$

$$= \frac{[\mu/(\mu + 1)]\, R_K}{R_K + [r_a/(\mu + 1)]}.$$

This can be compared with § 1.9.

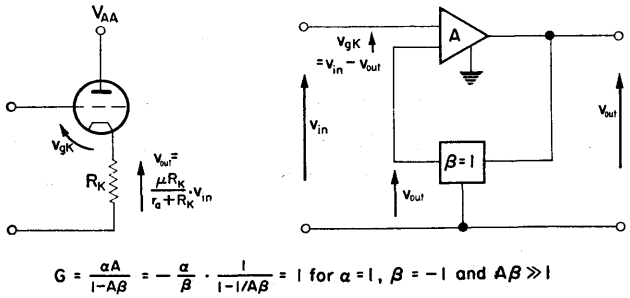



FIG. 7.5. Cathode follower as a feedback amplifier.

(b) *Current Amplifier*

A current amplifier with a fraction of the output current fed back in parallel with the input current has the property of low input impedance and high output impedance, together with a defined current gain. The outline of such an amplifier is shown in Fig. 7.6.

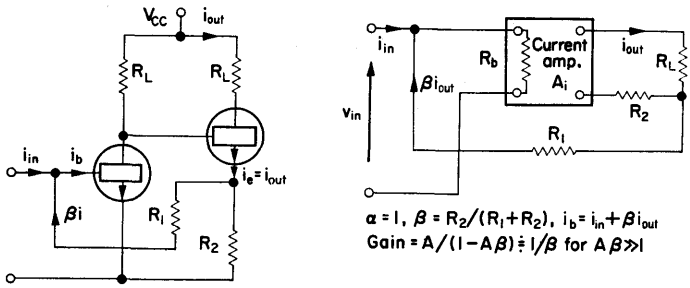



FIG. 7.6. Series–shunt feedback amplifier. There is no inversion in the amplifier but $\beta$ is negative. The emitter current, $i_{out}/h_{fb} \doteq i_{out}$ since $h_{fb}$ is very nearly unity.

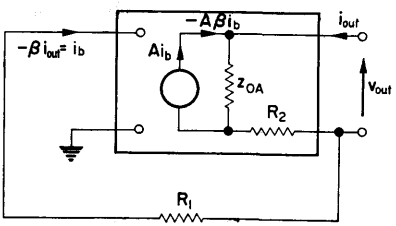



FIG. 7.7. Measurement of output impedance. The current $i_{out}$ is injected and $i_m$ is zero.

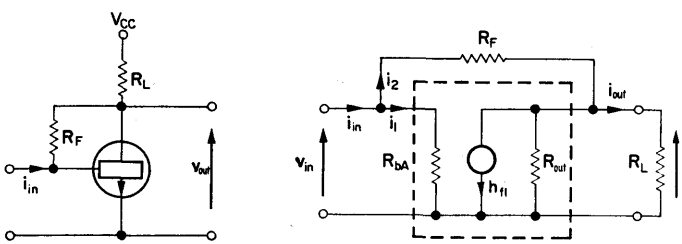



FIG. 7.8. Shunt–shunt feedback.

*Input impedance.*

$$z_{in} = \frac{v_{in}}{i_{in}}.$$

$$v_{in} = i_b R_b \text{ (from Fig. 7.6)}$$

$$= (i_{in} + \beta i_{out}) R_b$$

$$= i_{in}\left(1 + \frac{A\beta}{1 - A\beta}\right) R_b,$$

as

$$i_{out} = \frac{A}{1 - A\beta} i_{in} \text{ from eqn. (7.2),}$$

or

$$\frac{v_{in}}{i_{in}} = \frac{R_b}{1 - A\beta}.$$

Thus

$$z_{in} = \frac{R_b}{1 - A\beta}. \tag{7.7}$$

The input impedance of the $A$ amplifier is decreased by the factor $1/(1 - A\beta)$ for parallel input.

*Output impedance.* If current $i_{out}$ is injected and the input signal is zero, the output impedance,

$$z_{out} = \frac{v_{out}}{i_{out}} \quad \text{(see Fig. 7.7).}$$

If the feedback is zero ($R_2 = 0$) the output resistance is $z_{oA}$. If $\beta$ is not zero,

$$i_{out} - A\beta i_{out} = \frac{v_{out} - i_{out} R_2}{z_{OA}}.$$

Thus

$$z_{out} = (1 - A\beta)\, z_{oA} + R_2. \tag{7.8}$$

For negative feedback $(1 - A\beta)$ is greater than unity and the output resistance is thus increased by series (or current) feedback.

(c) *Shunt–shunt Feedback*

A signal proportional to the output voltage, fed back in parallel with the input signal, produces low input and output impedance together with a defined transfer impedance. Such a feedback arrangement is illustrated in Fig. 7.8.

$$v_{out} = Z_t i_1,$$

where $Z_t$ is the current gain times the shunt resistance $\doteqdot \dfrac{-h_f}{G_0 + G_L}$,

$$v_{out} = Z_t(i_{in} - i_2),$$

$$= Z_t\left(i_{in} - \frac{v_1 - v_{out}}{R_F}\right).$$

Therefore

$$\left(1 - \frac{Z_t}{R_F}\right) v_{out} = Z_t\left(i_{in} - \frac{i_1 R_b}{R_F}\right) \quad (\text{as } v_1 = i_1 R_b).$$

Substituting $i_1 = v_{out}/Z_t$ and rearranging,

$$\left(1 - \frac{Z_t - R_b}{R_F}\right) v_{out} = Z_t i_{in}.$$

Thus,

$$v_{out} = \frac{Z_t}{1 - [(Z_t - R_b)/R_F]}\, i_{in} \tag{7.9}$$

$$= \frac{-R_F}{1 - [(R_F + R_b)/Z_t]}\, i_{in}$$

$$\doteqdot \frac{-R_F}{1 - (R_F/Z_t)}\, i_{in} \quad (R_b \ll R_F), \tag{7.10}$$

and

$$\frac{v_{out}}{i_{in}} \doteqdot -R_F \quad (\text{for } Z_t \gg R_F). \tag{7.11}$$

*Input impedance,* $Z_{in}$.

$$\begin{aligned} i_{in} &= i_1 + i_2 \\ &= \frac{v_{in}}{R_b} + \frac{v_{in} - v_{out}}{R_F} \\ &= \frac{v_{in}}{R_b} + \frac{1 - (Z_t i_1 / v_{in})}{R_F} \\ &= v_{in}\left[\frac{1}{R_b} + \frac{1 - (Z_t/R_b)}{R_F}\right]. \end{aligned}$$

Therefore

$$\frac{v_{in}}{i_{in}} = \frac{R_b R_F}{R_F + R_b - Z_t}.$$

$$Z_{in} = \frac{R_b R_F/(R_F + R_b)}{1 - [Z_t/(R_F + R_b)]}.$$

For a transistor amplifier $R_b \ll R_F$, and

$$z_{in} = \frac{R_b}{1 - (Z_t/R_F)}. \tag{7.12}$$

EXAMPLE.

$h_f = 49$, $R_{out} = 20\ \text{k}\Omega$, $R_L = 5\ \text{k}\Omega$, $R_b = 2\ \text{k}\Omega$, $R_F = 50\ \text{k}\Omega$.

*A* amplifier transfer impedance:

$$Z_t = \frac{-h_f}{G_0 + G_L} = \frac{-49}{250 \times 10^{-6}} = -196\ \text{k}\Omega,$$

where the negative sign indicates signal inversion. Substituting values in eqn. (7.9),

$$\begin{aligned} v_0 &= \frac{-196\ \text{k}\Omega}{1 - [(-196\ \text{k}\Omega - 2\ \text{k}\Omega)/50\ \text{k}\Omega]} \cdot i_{in} \\ &\doteqdot \frac{200\ \text{k}\Omega}{1 + 4} \cdot i_{in} \quad \left(\text{as } \frac{Z_t}{R_F} \doteqdot 4\right) \\ &\doteqdot -40\ \text{k}\Omega \cdot i_{in}. \end{aligned}$$

Thus, in the presence of feedback, the transfer impedance is reduced.

*Input resistance*, $\frac{v_{in}}{i_{in}} \doteqdot \frac{2\,\text{k}\Omega}{1+4} = 400\ \Omega$ [from eqn. (7.12)]. As shown in (a), parallel feedback provides a low output impedance.

(d) *Series–series Amplifier*

A voltage proportional to the output current, fed back in series with the input, produces a high input impedance, high output impedance together with a defined transfer conductance. Two examples of this form of feedback are illustrated in Fig. 7.9.

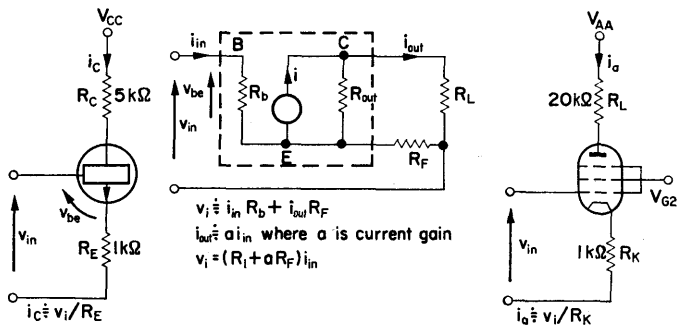



FIG. 7.9. Examples of series–series amplifier.

For the current amplifier,

$$i_{out} = Ai_{in}$$

$$= \frac{Av_{in}}{R_b + AR_F} \quad \text{(from Fig. 7.9)}$$

$$\doteqdot \frac{v_{in}}{R_F} \quad (\text{for } R_b \ll AR_F).$$

$$R_{in} = R_b + AR_F$$

$$\doteqdot AR_F \quad \text{for} \quad R_b \ll AR_F. \qquad (7.13)$$

As shown in (b), series output feedback provides a high output impedance.

EXAMPLES.

1. Transistor with emitter resistor. By the above reasoning

$$i_c = \frac{v_{in}}{R_E} = \frac{v_{in}}{10^3} \quad \text{in the example of Fig. 7.9.}$$

$$v_c = -AR_C i_{in}, \quad \text{where the current gain, } A = \frac{h_{fe}G_C}{G_E + G_C},$$

$$= -\frac{AR_C}{r_{in}} v_{in} \quad \text{where} \quad r_{in} \doteqdot AR_E.$$

Thus voltage gain,

$$\frac{v_c}{v_{in}} = -\frac{R_C}{R_E} \doteqdot -\frac{5\,\text{k}\Omega}{1\,\text{k}\Omega}$$

in this example.

2. For the pentode of Fig. 7.9,

$$i_a = \frac{v_{in}}{r_a + R_L + (\mu + 1) R_K}$$

$$\doteqdot \frac{g_m}{1 + g_m R_K} \cdot v_{in} \quad (\text{for } r_a \gg R_L)$$

$$\doteqdot \frac{v_{in}}{R_K} \quad (\text{for } g_m R_K \gg 1).$$

Thus, voltage gain,

$$\frac{-i_a R_L}{v_{in}} \doteqdot \frac{-R_L}{R_K}.$$

If the pentode is operated with

$$g_m = 10\,\text{mA/V}, \quad r_a = 1\,\text{M}\Omega,$$

$$\text{the transfer conductance} = \frac{10^{-3}}{1 + (10 \times 10^{-3} \times 10^{-3})}$$

$$\doteqdot \frac{1}{R_K} = 1 \text{ mA/V}.$$

$$\text{Voltage gain} \doteqdot -\frac{R_L}{R_K} \doteqdot -20.$$

(e) *Computing Amplifier*

This is a form of shunt–shunt feedback, and is shown in Fig. 7.10. From (c), $v_{out} = -Z_F i_{in}$ (where $Z_F$ is the feedback impedor), provided the $A$ amplifier transfer impedance $Z_t \gg Z_F$.

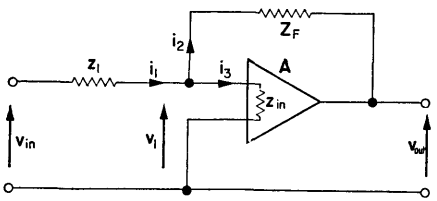



FIG. 7.10. Computing amplifier. For a voltage operated amplifier $Z_{in}$ will be very large, while for a current amplifier $Z_{in}$ will be small.

With an external input impedor $Z_1$, because of the low input impedance to the amplifier with feedback, an input current $i_{in} = v_{in}/Z_1$ will flow. Thus,

$$v_{out} = -\frac{Z_F}{Z_1} \cdot v_{in}. \tag{7.14}$$

If $A$ is a voltage amplifier, eqn. (7.2) can be used and $i_3$ neglected. Thus,

$$v_{out} = \frac{\alpha A}{1 - A\beta} v_{in}.$$

In Fig. 7.11, $\alpha v_{in}$ is the voltage at the summing point of the amplifier when the output is short circuited:

$$\alpha = \frac{Z_F}{Z_1 + Z_F}. \tag{7.15}$$

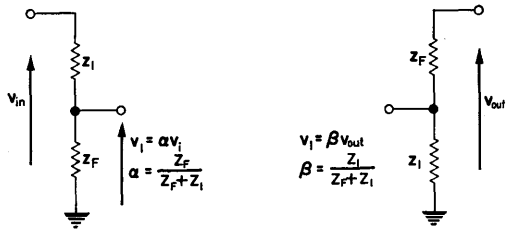



FIG. 7.11. Determination of $\alpha$ and $\beta$.

$\beta v_0$ is the voltage produced at the summing point of the amplifier by the output, when the input is short circuited:

$$\beta = \frac{Z_1}{Z_1 + Z_F}. \tag{7.16}$$

Thus, substituting for $\alpha$ and $\beta$,

$$v_{out} = \frac{[Z_F/(Z_1 + Z_F)]\,A}{1 - [Z_1/(Z_1 + Z_F)]\,A}\, v_{in}$$

$$= -\frac{Z_F}{Z_1} \cdot \frac{1}{1 - (1/A\beta)} \cdot v_{in}$$

$$\left(\text{where } A\beta = A \cdot \frac{Z_1}{Z_1 + Z_F}\right) \tag{7.17}$$

$$= -\frac{Z_F}{Z_1} v_{in} \quad \text{for} \quad A\beta \gg 1. \tag{7.18}$$

If $i_3$ cannot be neglected (as in the case of a transistor amplifier), $i_1 = i_2 + i_3$.

Therefore

$$\frac{v_{in} - v_1}{Z_1} = v_1\left(\frac{1}{z_{in}} + \frac{1}{Z_F}\right) - \frac{v_{out}}{Z_F},$$

or

$$Y_1 v_{in} = \frac{v_{out}}{A}(y_{in} + Y_F + Y_1 - AY_F),$$

and

$$v_{out} = \frac{Y_1}{Y_F}\left[\frac{Av_{in}}{(1 - A) + (Y_1 + y_{in})/Y_F}\right]$$

$$= -\frac{Y_1}{Y_F}\left[\frac{v_{in}}{1 - (Y_1 + y_{in} + Y_F)/AY_F}\right]. \quad (7.19)$$

This is the same form as eqn. (7.17) but with

$$\beta = \frac{Y_F}{Y_1 + y_{in} + Y_F} = \frac{Z_1 z_{in}/(Z_1 + z_{in})}{(Z_1 z_{in}/(Z_1 + z_{in})] + Z_F}.$$

It is apparent that $\beta$ is formed by $Z_1$ and $z_{in}$ in parallel, in series with feedback impedance $Z_F$. With valve amplifiers $z_{in}$ is, in many cases, sufficiently large to be ignored and then the loop gain expression is

$$A\beta = \frac{AZ_1}{Z_1 + Z_F}$$

as in eqn. (7.17).

EXAMPLE. Let $A = -100$, $Z_1 = 100\,\text{k}\Omega$, $Z_F = 1\,\text{M}\Omega$. Then

$$\beta = \frac{100\,\text{k}\Omega}{100\,\text{k}\Omega + 1\,\text{M}\Omega} = \frac{1}{11},$$

and

$$A\beta = -9{\cdot}1.$$

$$\frac{v_{out}}{v_{in}} = G = -\frac{Z_F}{Z_1}\frac{1}{1 - (1/A\beta)} = -10\,\frac{1}{1 + (1/9{\cdot}1)}$$

$$= -10\,\frac{1}{1{\cdot}11} = -9.$$

Thus, the percentage error involved in expressing $v_{out}/v_{in} = -Z_F/Z_1$ is approximately $100/A\beta\%$. In this example it is 11%.

*Low input impedance amplifier.* The conventional transistor amplifier has a low input impedance in contrast to the high input impedance of the valve amplifier. (There are semiconductor devices such as field effect transistors with high input impedance.)

Considering eqn. (7.19),

$$v_{out} = -\frac{Y_1}{Y_F}\frac{v_{in}}{1 - [(Y_1 + y_{in} + Y_F)/A_v Y_F]}$$

$$= -\frac{Y_1}{Y_F}\frac{v_{in}}{1 - \{1 + [(Y_1 + Y_F)/y_{in}]/(A_v Y_F/y_{in})\}}.$$

The voltage gain of an amplifier can be expressed as

$$A_v = \frac{A_i R_L}{z_{in}} = \frac{A_i y_{in}}{Y_L} = Z_t y_{in},$$

where $Y_L$ is the effective load admittance and $Z_t$ is the transfer impedance of the amplifier. Thus,

$$v_{out} = -\frac{Y_1}{Y_F}\frac{v_{in}}{1 - \{1 + [(Y_1 + Y_F)/y_{in}]/Z_t Y_F\}} \qquad (7.20)$$

$$= -\frac{Z_F}{Z_1}\left[\frac{v_{in}}{1 - (Z_F/Z_t)}\right] \quad (\text{if } y_{in} \gg Y_1 + Y_F). \qquad (7.21)$$

EXAMPLE. Let $Z_t = -1\,\text{M}\Omega$. The negative sign indicates that a current flowing into the amplifier causes a negative output voltage. For this transfer impedance, an input current of $1\,\mu\text{A}$ produces an output voltage of $-1\,\text{V}$.

If

$$R_F = 100\,\text{k}\Omega, \quad r_{in} = 1\,\text{k}\Omega \quad \text{and} \quad R_1 = 10\,\text{k}\Omega,$$

using eqn. (7.21),

$$G = \frac{v_{out}}{v_{in}} = -10\,\frac{1}{1 + 0{\cdot}11} = 9{\cdot}01.$$

The error in expressing the gain as $-Z_F/Z_1$ is approximately $(Z_t/Z_F)\,.\,100\%$.

For high accuracy it is required that $Z_t \gg Z_F$ and $r_{in} \ll Z_1 Z_F/(Z_1 + Z_F)$.

Because the loop gain of the low input impedance amplifier is largely independent of $Z_1$, this type of amplifier has advantages over the high input impedance amplifier where the loop

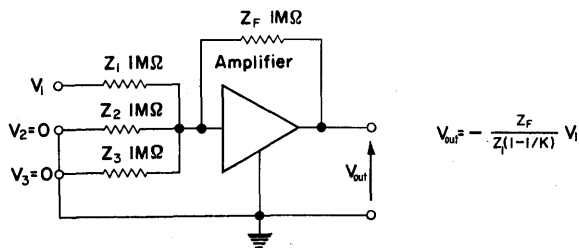
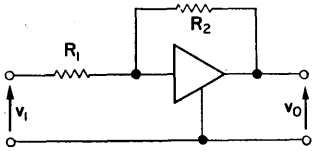



FIG. 7.12. Effect of input resistors on computing amplifier performance. For a high input impedance amplifier, having voltage gain $A$, $K = A[Y_F/(Y_F + \Sigma Y_1)]$. The effect of $Z_2$ and $Z_3$ is to reduce the loop gain from $A/2$ to $A/4$. For a low input impedance amplifier, $K = Z_T Y_F$, which is indepedent of $\Sigma Y_1$, the parallel combination of the input impedors.

gain is $AZ_1/(Z_1 + Z_2)$. In the latter case, if the amplifier is to be used to provide voltage gain, the loop gain, and consequently the accuracy of computation, are reduced together with the bandwidth. In the former case, for a given $Z_F$, the bandwidth and accuracy of computation are ideally constant. (See Fig. 7.12.)

Some simple operations using computing amplifiers are shown in Fig. 7.13.

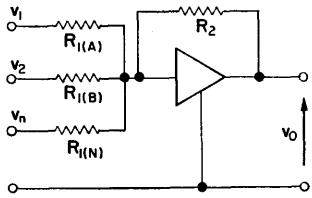
For further applications, reference should be made to standard works on analogue computing. Figure 7.14 illustrates the input and output waveforms of a computing amplifier when used as an integrator.




(a) Single inverter

$$\frac{v_0}{v_1} = -\frac{R_2}{R_1} \left\{ \begin{matrix} \text{For } A\beta \gg 1 \\ \text{or } Z_1 \gg R_2 \end{matrix} \right.$$

$v_0 = -v_1$ for $R_2 = R_1$

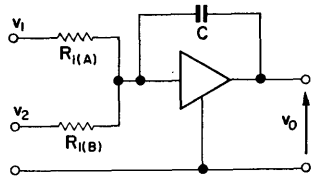



(b) Adder

$$v_2 = -R_2 \left[ \frac{v_1}{R_{1(A)}} + \frac{v_2}{R_{1(B)}} \cdots + \frac{v_n}{R_{1(N)}} \right]$$

$$= -(v_1 + v_2 \cdots + v_n)$$

For $R_2 = R_{1(A)} = R_{1(B)} \cdots = R_{1(N)}$




(c) Integrator

$$v_0(s) = \frac{v_1}{sCR_{1(A)}} - \frac{v_2}{sCR_{1(B)}}$$

$$v_0(t) = -\frac{1}{CR_{1(A)}} \int_0^t v_1 \, dt - \frac{1}{CR_{1(B)}} \int_0^t v_2 \, dt$$

FIG. 7.13. Applications of computing amplifiers. The input to the *A* amplifier is frequently referred to as the summing point.

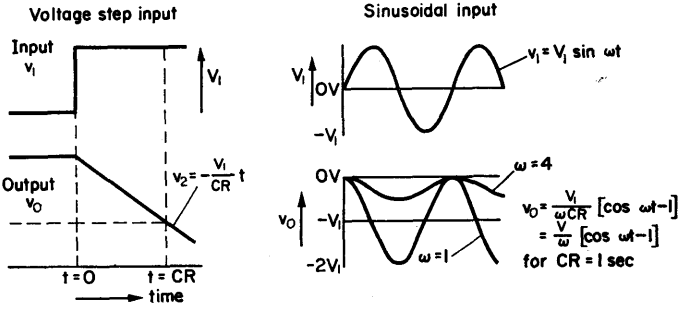



FIG. 7.14. Response of an integrator to a step function and sine wave input.

## 7.3. Application of Negative Feedback to Stabilize Transistor Operation

Because of the wide spread of transistor parameters, it is necessary in some applications to use local feedback loops within the over-all feedback system.

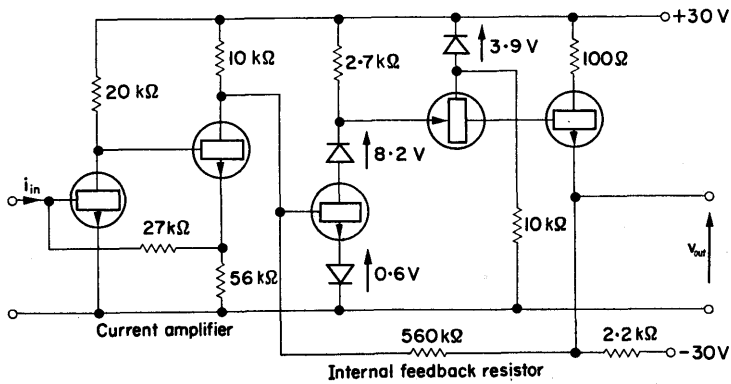



FIG. 7.15. Amplifier with transfer resistance of $-250$ MΩ. The common base stage gives high voltage gain and allows the output voltage to swing positively and negatively. Stabilizing elements are not included.

EXAMPLE. Computing amplifier with defined internal transfer impedance of $-250$ MΩ.

The amplifier consists of a current amplifier (type b in Fig. 7.2) with a defined gain of 500, and a shunt–shunt stage (type c) with 0·5 MΩ feedback resistor.

The over-all transfer impedance is

$$Z_t = 500 \times -0{\cdot}5\ \text{M}\Omega = -250\ \text{M}\Omega.$$

When used in a computing system with a feedback resistor $R_F = 100$ kΩ,

$$v_{out} = \frac{-R_F}{1 - R_F/Z_t} \cdot i_{in} = -R_F i_{in}$$

to an accuracy of 0·025%. Such an amplifier is illustrated in Fig. 7.15.

Apart from standardizing the gain, the local feedback has the following features.

(a) The shunt feedback across the input stage gives a low input impedance which is desirable for computing purposes. (See § 7.2.)
(b) Similarly, the input impedance to the second feedback loop is low. This allows efficient current transfer from the first loop to the second.
(c) The voltage or shunt feedback from the output reduces the amplifier output impedance below that of the emitter follower. In computing systems a low output impedance is necessary.

## 7.4. Stability of Amplifiers with Negative Feedback

Although at signal frequencies an amplifier may be operating with negative feedback applied, at frequencies above the operating range (and below the operating range in the case of a capacitor or transformer coupled amplifier) the feedback may become positive due to phase change in the loop gain.

The gain with feedback, $G = \alpha A/(1 - A\beta)$ [from eqn. (7.2)], where the loop gain $A\beta$ is negative for negative feedback. If $A\beta$ becomes positive and equal to or greater than unity, $G$ will tend to infinity and the amplifier will oscillate. (See Chapter 9.)

Thus, a condition for stability is that the loop gain (a vector quantity) should always be less than unity, or $A\beta < 1$. ($A\beta$ is a phasor having magnitude $|A\beta|$ and angle $\measuredangle\theta$ as in Fig. 7.16.)

Consider an amplifier with gain $A_0$ of $-1000$ and a feedback fraction $\beta$ equal to 0·01. The loop gain, $A_0\beta = -10$. If $\beta$ is independent of frequency, and the amplifier is a zero frequency type, the loop gain locus follows the $A$ locus as shown in Fig. 7.16. The amplifier shown is stable, since $(1 - A\beta)$ is always greater than zero as the phasor moves around the locus.

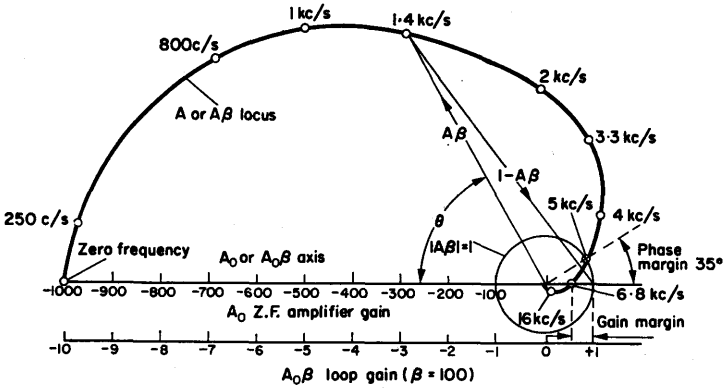



FIG. 7.16. Polar plot of a three-stage z.f. amplifier modified to show the loop gain locus. The $\beta$ network is independent of frequency. The amplifier is stable as $A\beta$ is always less than unity, since it never encloses or passes through the point $+1$ on the $A_0\beta$ axis.

### *Phase and Gain Margin*

An indication of the stability of an amplifier is the phase angle between the input signal and the $A\beta$ phasor at the frequency where $A\beta = 1$. This is the *phase margin.* A typical value is of the order of 45° to ensure stability under all conditions. If the locus passes through the point $+1$ on the $A_0\beta$ axis, the phase margin is zero and the amplifier will oscillate at the frequency indicated on the locus. If the locus encloses the point $+1$ on the $A_0\beta$ axis, the amplifier will in general be unstable and will oscillate at approximately the frequency at which the $A\beta$ locus intersects the $A_0\beta$ axis (i.e. the frequency at which the angle of $A\beta$ is 180° with respect to $A_0\beta$).

Alternatively, the degree of stability can be specified by the *gain margin.* This is $1 - A\beta$ when the phase shift of $A\beta$ is 180°. The gain margin will be zero if the locus passes through $+1$ on the $A_0\beta$ axis, or negative if the $A\beta$ locus encircles the point. In Fig. 7.16, the loop gain $|A\beta|$ is 0·55 and $1 - A\beta$ is 0·45 when

$\theta = 180°$. This is the gain margin and is positive for a stable system.

Gain margin can be given in logarithmic form as G.M. (dB) $= 20 \log_{10} \left| \frac{1}{A\beta(180°)} \right|$ where $A\beta$ (180°) is the loop gain at the frequency at which the $A\beta$ locus intersects the $A_0\beta$ axis. In the above example the gain margin is +5 dB. For an unstable system the gain margin will be zero or negative.

*Closed Loop Performance*

$$G = \frac{\alpha A}{(1 - A\beta)} = -91$$

at zero frequency.

The amplitude and phase response of the above amplifier can be obtained from consideration of the $A\beta$ locus. If $\alpha = 1$, $G$ is the ratio of the phasors $A$ and $1 - A\beta$.

Figure 7.17 is constructed by measuring the magnitude of $A$ and $1 - A\beta$ at various frequencies and determining $G = \frac{A}{1 - A\beta}$.

*Bandwidth Extension*

The bandwidth is increased by approximately $1 - A_0\beta$, but there is an increase in gain above $G_0$ as the locus passes near the point +1 on the $A_0\beta$ axis. If the loop gain $A\beta$ is increased, the peak is increased and will go off to infinity when the locus passes through +1 on the axis.

*Logarithmic Representation*

This is a very useful approach for feedback amplifier design as the frequency response of the $A$ amplifier can be readily obtained from straight line asymptote approximation (§ 3.3). The ordinate is calibrated in relative gain. A horizontal line can be drawn corresponding to the loop gain. In Fig. 7.18, $A_0\beta = 10$ (or 20 dB), and the gain margin and phase margin can be read

off immediately. If the loop gain is increased to 40 dB, the unity loop gain line will be at −40 dB, giving a negative phase margin of 60° and a negative gain margin of 15 dB. The system will oscillate at a frequency of approximately 7 kc/s.

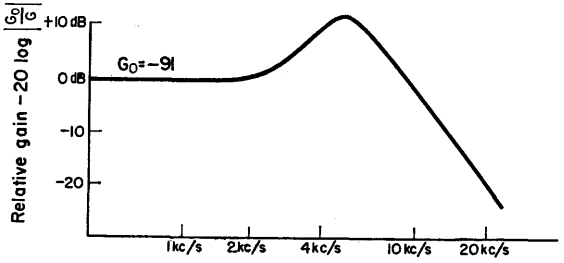



FIG. 7.17. Amplitude-frequency plot for closed loop performance of the amplifier of Fig. 7.16. Note the peak in response as the $A\beta$ locus approaches the point −1 on the $A_0\beta$ axis.

*Stabilization of Feedback Amplifiers.*

Amplifiers incorporating one valve or transistor will usually be stable, but will possibly have peaks in the amplitude response. Multistage amplifiers involving three or more amplifying devices will be unstable in most cases, when feedback is applied. The example of Fig. 7.18 is only stable with a relatively low degree of feedback (21 dB). If the degree of feedback is increased to 26 dB the system will oscillate.

$$\text{Degree of feedback} = \frac{\text{gain without feedback}}{\text{gain with feedback}}$$

$$= 20 \log_{10}(1 - A_0\beta). \qquad (7.22)$$

*Control of Attenuation*

Instability is caused by the phase shift becoming 180° before the loop gain has become unity. Each breakpoint introduces 45° phase shift at the break frequency tending to 90° at infinite frequency, as is shown in Fig. 3.7. If there is only one breakpoint

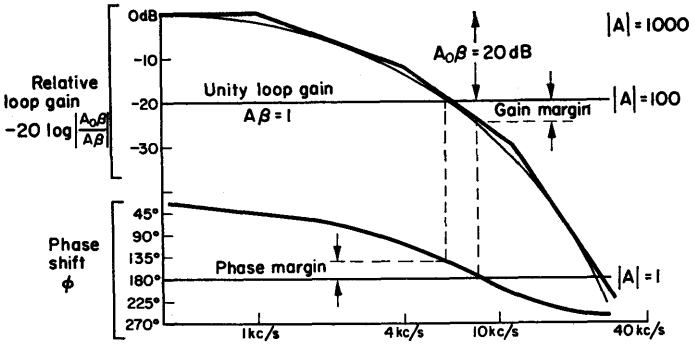



FIG. 7.18. Loop gain plotted on logarithmic axes. $|A_0\beta| = 10$ (or 20 dB).

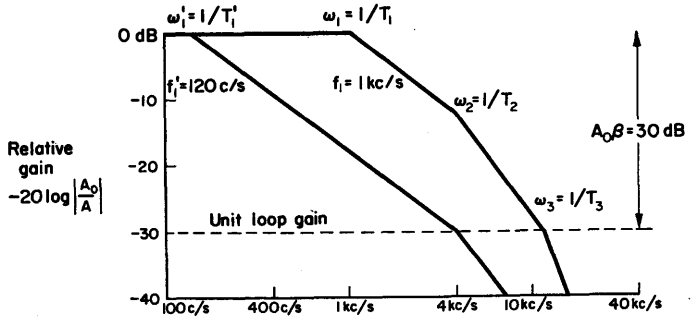



FIG. 7.19. Control of attenuation out to the frequency at which loop gain is unity. Bandwidth of $A$ amplifier is reduced from 1 kc/s to 120c/s. $T_1 = 0{\cdot}16 \times 10^{-3}$ sec is increased to $T_1 = 1{\cdot}3 \times 10^{-3}$ sec.

between the frequency at which the loop gain becomes unity and the midband frequency, the phase shift will have a maximum value of 135° and the system will be stable with a phase margin of 45°.

The simplest way of accomplishing a controlled attenuation is to have one time constant much larger than the others (see Fig. 7.19). This controls the fall off in gain until further phase

shift, introduced by the other time constants, can be permitted. To enable a loop gain of 30 dB to be used, the time constant $T_1$ can be increased so that the gain falls at 6 dB/octave to the breakpoint at 4 kc/s. The phase shift at unity loop gain is 140° giving a phase margin of 40°. The open loop bandwidth is reduced from 1 kc/s to 120 c/s.

## 7.5. Performance of an Amplifier with Parallel Feedback

Example. The capacitor coupled amplifier of Fig. 3.26, using a 6AU6 pentode and cathode follower output is employed. A blocking capacitor is used to isolate the feedback network from the cathode follower output.

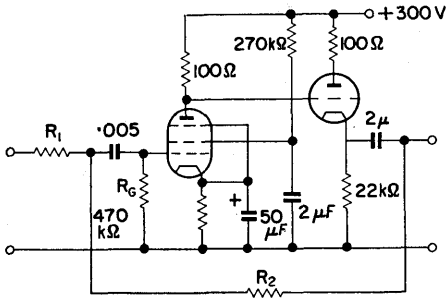



Fig. 7.20. Amplifier of Fig. 3.26 with feedback applied.

*Signal inverter.* When used as a signal inverter as in Fig. 7.20, $R_1 = R_2$ and

$$\beta = \frac{R_1}{R_1 + R_2} = \tfrac{1}{2},$$

$$\alpha = \frac{R_2}{R_1 + R_2} = \tfrac{1}{2}.$$

The loop gain

$$A_0\beta = \frac{-220}{2} = -110, \quad 1 - A_0\beta = 111.$$

Percentage error $\doteqdot \dfrac{100}{A_0\beta} = 0{\cdot}91\%.$

The high loop gain produces a wide bandwidth, but additional phase shift produced by the feedback network causes peaking at the h.f. end (see Figs. 7.21 and 7.22).

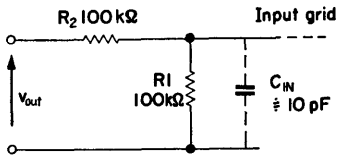



FIG. 7.21. Extra lag introduced by feedback network.

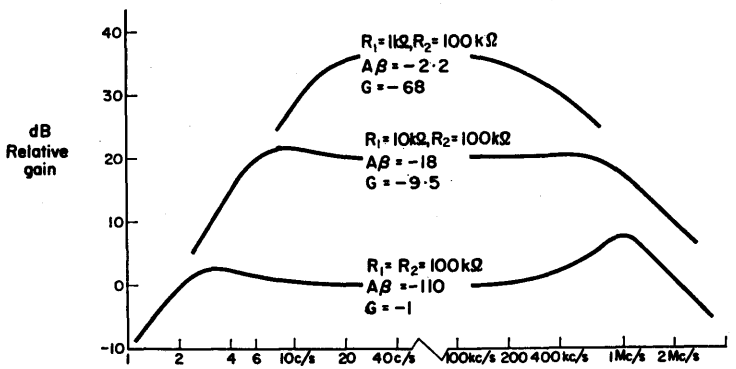



FIG. 7.22. Amplitude response for the amplifier of Fig. 7.20. Note the break in the frequency axis.

The peak at low frequency can be eliminated by increasing $C_C$, the coupling capacitor, to 1 $\mu F$. This ensures that the gain falls off steadily at 20 dB/decade.

Resistance at summing point $\doteqdot \dfrac{R_2}{1 - A_0} \doteqdot 450\,\Omega$

Output resistance $= \dfrac{R_0}{1 - A_0\beta} \doteqdot 3\,\Omega$

} values at mid-band.

The foregoing analysis assumes zero source and load impedance.

*Voltage amplifier.* For a nominal gain of $-10$, $R_1 = 10\,\text{k}\Omega$ and $R_2 = 100\,\text{k}\Omega$. The loop gain is reduced to $-18$ and the error is increased to 5%.

## 7.6. High Input Resistance Amplifier

Series–series feedback enables a high input resistance to be produced by reducing the voltage across the input to the $A$ amplifier.

### Design Example 7.1

Required, a voltage amplifier with a gain of $-40$ and an input resistance of 10 MΩ, as in Fig. 7.23.

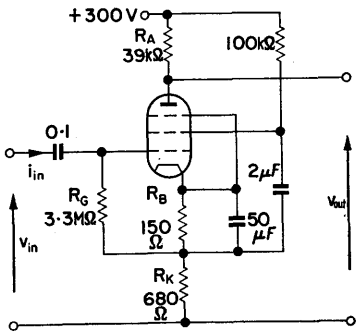



FIG. 7.23. High input resistance amplifier.

The manufacturer gives the following information for the 6AU6 valve.

For

$$V_{GK} = -1\text{ V},$$
$$V_A = 100\text{ V}, \quad I_A = 5\text{ mA},$$
$$V_S = 100\text{ V}, \quad I_S = 2{\cdot}1\text{ mA},$$
$$g_m = 3{\cdot}9\text{ mA/V},$$

and

$$r_a = 0{\cdot}5\text{ MΩ}.$$

The total cathode current operating under the above conditions is $I_A + I_S = 7{\cdot}1$ mA.

The cathode bias resistor, to give a $V_{GK} = -1$ V, is

$$R_B = \frac{1\text{ V}}{7{\cdot}1\text{ mA}} = 141\,\Omega.$$

Let

$$R_B = 150\,\Omega.$$

*Grid resistor.* The maximum value for the grid leak is 3·3 MΩ. This is the figure usually quoted by the manufacturer as the largest safe value because of grid current effects.

*Input resistance.* To increase the input resistance from the 3·3 MΩ of the grid resistor to the required 10 MΩ, the voltage across $R_G$ should be $\frac{3{\cdot}3}{10} v_{in}$ since

$$r_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{in} R_G}{(v_{in} - v_R)} \quad \text{(where } v_R \text{ is the voltage across } R_K \text{ in Fig. 7.23)}$$

$$= \frac{R_G}{1 - A_K} \quad \left(\text{where } A_K = \frac{v_R}{v_{in}}\right).$$

Thus,

$$A_K = \frac{r_{in} - R_G}{r_{in}} = 0{\cdot}7.$$

*Cathode resistor $R_K$.*

$$A_K = \frac{\mu R_K}{r_a + R_L + (\mu + 1) R_K} \quad \text{(from eqn. (1.13)]}$$

$$= \frac{g_m R_K}{1 + (R_L/r_a) + g_m R_K} \doteqdot \frac{g_m R_K}{1 + g_m R_K}$$

(for $R_L \ll r_a$).

Rearranging,

$$R_K = \frac{A_K}{g_m(1 - A_K)} = \frac{0{\cdot}7}{3{\cdot}9 \times 10^{-3} \times 0{\cdot}3} = 600\,\Omega.$$

Let $R_K$ be 680 Ω to ensure that the required input resistance is attained.

*Screen resistors.* For an anode supply of 300 V a screen resistor of 100 kΩ will provide a screen voltage of 100 V, if the screen current is 2 mA.

The decoupling capacitor should be returned to the cathode and not to the common terminal or the gain will be reduced by the inverse of $v_R$ being applied to the screen grid.

*Anode resistor.*

$$A \doteq \frac{-g_m R_L}{1 + g_m R_K} \quad \left(\text{for } \frac{R_L}{r_a} \ll 1\right)$$

or,

$$R_L = \frac{-A(1 + g_m R_K)}{g_m} = \frac{40(1 + 2{\cdot}65)}{3{\cdot}9 \times 10^{-3}} = 37{\cdot}4\,\text{k}\Omega.$$

Let

$$R_L = 39\,\text{k}\Omega.$$

## 7.7. High Input Resistance Transistor Amplifier as an Impedance Changer

A transistor amplifier, operating in common emitter, has an input resistance of the order of 1 kΩ. It has been shown that this can be decreased by shunt feedback or increased by series feedback.

The emitter follower uses series feedback, and, as shown previously, has a high input resistance and low output resistance. This enables it to be used for transformation from a high impedance level to a low level. An example of such an application is the computing amplifier of Fig. 7.15. The high impedance level of the output of a common base stage is transformed to the

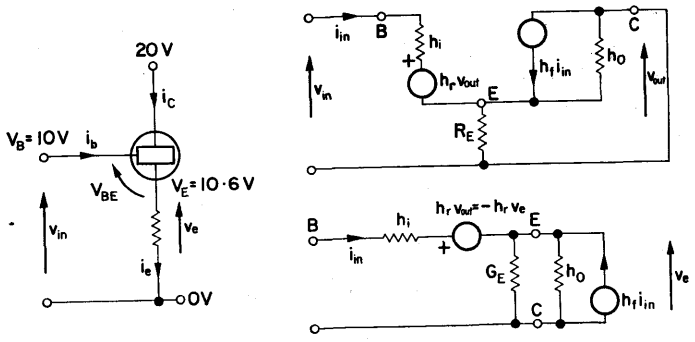



FIG. 7.24. Common collector amplifier (or emitter follower). For $V_B = -10$ V, $V_E \doteqdot 9{\cdot}4$ V for a silicon transistor and $V_{EB} \doteqdot 0{\cdot}6$ V.

low impedance required for the output of the computing amplifier, which should approximate to a voltage source.

From Fig. 7.24 it is apparent that the input voltage

$$v_{in} = v_{be} + v_e \doteqdot v_e \quad \text{(as } v_{be} \text{ is small)}.$$

EXAMPLE.

$$g_m = 40 \text{ mA/V} \quad \text{at} \quad I_C = 2 \text{ mA}.$$

The emitter current,

$$I_E = I_C + I_B \doteqdot I_C \quad \text{for} \quad h_f \gg 1.$$

For

$$v_e = 5 \text{ V} \quad \text{and} \quad R_E = 5 \text{ k}\Omega, \quad i_e = 1 \text{ mA},$$

and

$$v_{be} = \frac{i_c}{g_m} = \frac{1 \text{ mA}}{40 \text{ mA/V}} = 0{\cdot}025 \text{ V}.$$

The input signal is thus

$$v_{in} = v_{be} + v_e = 5{\cdot}025 \text{ V}.$$

The voltage difference between input and output is 0·025 V. In Fig. 7.24, the equivalent network shows that the voltage

difference is due to the input current $i_{in}$ flowing in $h_i$, with the term $h_r v_{out}$ having little effect because of the smallness of $h_r$.

The input resistance appears large because, for a current $i_{in}$ flowing into the base, a current $(1 + h_f)\, i_{in}$ flows into $(G_E + h_o)$.

Neglecting $h_r v_0$,

$$r_{in} = \frac{v_{in}}{i_{in}} = h_i + \frac{1 + h_f}{G_E + h_0} \doteqdot \frac{h_f}{G_E} \quad \text{(for large } h_f \text{ and } G_E\text{)}$$

$$\doteqdot 100 \times 5\ \text{k}\Omega \doteqdot 500\ \text{k}\Omega \quad \text{(for } h_f = 100\text{)}.$$

The greater current gain provided by the Darlington connection of Fig. 7.25 increases the input resistance.

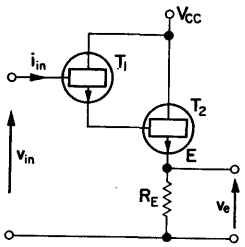



FIG. 7.25. Emitter follower using the Darlington connection. The base–emitter voltage of the combination is of the order of 1·2 V for silicon transistors.

*Example of Direct Coupled Emitter Follower (Darlington connection)*

The input current

$$I_{IN} = \frac{V_{IN} - V_{BE}}{BR_E} \quad \left(\text{where } B \doteqdot (h_{FE})^2\right).$$

For

$$V_{IN} = 5\ \text{V}, \quad R_E = 1\ \text{k}\Omega \quad \text{and} \quad h_{EE} = 50,$$

$$I_{IN} \doteqdot \frac{4\ \text{V}}{2500 \times 1\ \text{k}\Omega} = 1{\cdot}6\ \mu\text{A}.$$

Such an amplifier will draw only a small current from the previous stage, whereas a single transistor emitter follower would require nearly 50 times the input current. $T_1$ is operated at a low current level and its current gain will be somewhat less than its quoted value (see Fig. 7.26).

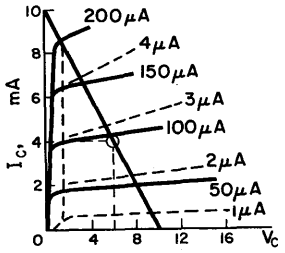



FIG. 7.26. Curves for a Darlington connected transistor (broken line) and a single transistor (solid line), plotted for silicon planar devices which provide current gain at low current levels. The single transistor requires 80 μA to supply 4 mA emitter current compared with 2·7 μA required by the compound device.

*Capacitor Coupled Emitter Follower* (Fig. 7.27)

For capacitor coupling some bias arrangement is necessary. The common forms of biasing will reduce the input resistance.

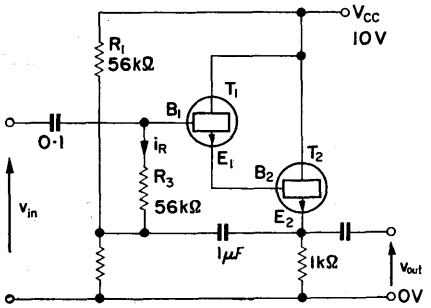



FIG. 7.27. High input impedance emitter follower. The effective value of $R_3$ is increased by the feedback connection.

F-G/E. 9a

By utilizing the small change in $V_{BE}$ with collector current, the external base–emitter impedance can be increased. Bias is supplied to $T_1$ by the bias network $R_1$, $R_2$ and $R_3$. The latter can be relatively large as the leakage current for the silicon planar transistors is small.

At signal frequencies $R_3$ is effectively across $B_1E_2$.

The voltage across $R_3$,

$$v_{b1e2} = v_{\text{in}} - v_{\text{out}}.$$

The internal voltage gain,

$$A_v = \frac{v_{\text{out}}}{v_{b1e2}}.$$

$$i_R = \frac{v_{b1e2}}{R_3} = \frac{v_{\text{in}} - v_{\text{out}}}{R_3} = \frac{v_{\text{in}} - [Av_{\text{in}}/(1 + A)]}{R_3}$$

$$= \frac{v_{\text{in}}}{(1 + A)\,R_3}.$$

The effective value of $R_3 = (1 + A)\,R_3$, where $A$ is several hundred. Thus the effect of $R_3$ will be small and the input impedance will be principally determined by $h_f^2 R_E$.

## 7.8. Direct Coupled Amplifier with Feedback

The zero frequency amplifier of Design Example 6.4 is intended for use as a feedback amplifier for computing purposes. There are two main breakpoints due to the pentode and longtail pair stages. Two further breakpoints are due to (a) the cathode follower output stage, and (b) the capacitance at the summing point.

The capacitances $C_{OP}$ and $C_{SP}$ in Fig. 7.28 can be considerable, and vary with different applications. A small capacitor $C$ is sometimes employed to reduce the effect of $C_{SP}$ in the same way as capacitance is introduced in resistive coupling networks (see § 6.3). This additional capacitor, however, reduces the overall closed loop bandwidth (see Fig. 7.30).

From the above considerations it is apparent that the amplifier will be unstable when feedback is applied, as the effective input and output capacitances will introduce phase shift additional to the maximum internal phase shift of 180°.

With 100 kΩ input and feedback resistors the amplifier oscillates at 140 kc/s producing a large amplitude sawtooth waveform. This indicates that a phase shift of 180° is produced at

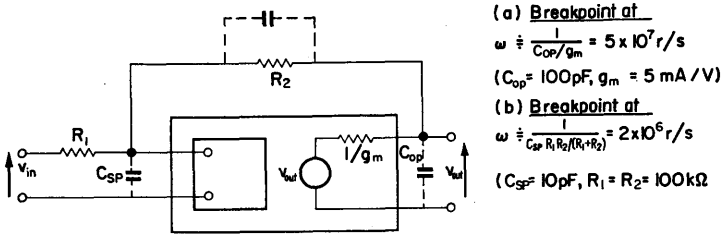



FIG. 7.28. Introduction of two lags at high frequency by capacitance at the output and summing points.

approximately 140 kc/s where the loop gain is considerably in excess of unity, i.e. the large non-linear waveform is caused by a large negative gain margin.

*Stabilization*

In the absence of any special considerations, a reasonable approach is to ensure that there is only one breakpoint above the unity gain line (when $\beta = 1$), and that the second breakpoint lies on the unity gain line. This implies that the internal phase shift is 135° at unity gain when all the output signal is fed back to the input. In most cases this will be sufficient for stability. If it is not, the second breakpoint can be made to occur below unity gain. On the other hand, if $\beta$ is always to be small, it may be possible to introduce the second breakpoint above unity gain.

Two simple methods of stabilization will be considered. Both involve the reduction of open loop bandwidth which is always

inevitable in the stabilization of multistage amplifiers. The gain asymptote is controlled by modifying the breakpoint of one or more stages. In the interest of maximum bandwidth it is desirable to modify the stage with the lowest breakpoint (in the example this is the pentode stage), but if large signals are required to be handled at high frequencies, the final voltage amplifier stage should not be modified. This is because the stage can only accept a relatively small amplitude signal (of the order of 1 V) between the conditions of grid cut-off and anode bottoming. At high frequencies, the gain of this stage is reduced but the amplifier, in feedback connection, still demands the same amplitude output signal. Consequently, the stage is supplied with a larger input signal and this will cause overloading at some frequency. The output waveform will thus be distorted, unless the amplitude of the input signal is reduced.

In this example, signal handling will be better if the input stage is modified, as it has to produce only a small output signal. However, the overall bandwidth will be greater if the pentode stage is modified. The latter course will be adopted.

*Dominant Lag Stabilization*

The lag introduced by the pentode is increased so that the gain falls to unity before the breakpoint of the longtail pair occurs. The required breakpoint for the pentode can be found by projecting back from the intercept of the unity gain line and $f_2$ (the frequency of the L.T.P. breakpoint), at a slope of 20 dB/decade. The frequency at which this projection meets the 0 dB relative gain line is the required breakpoint $f_1'$. From Fig. 7.29, $f_1'$ is 20 c/s,

and
$$\omega_1' = 2\pi f_1',$$

$$T_1' = \frac{1}{\omega_1'} = C_d R$$

(where $C_d R$ is the required dominant lag, and $R$ is the effective shunt resistance = 0·8 MΩ).

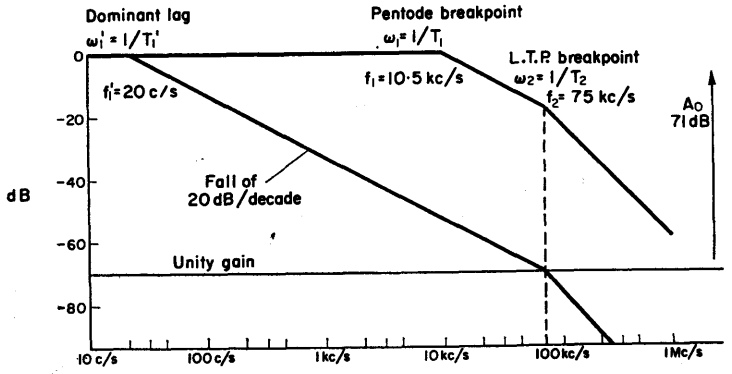



FIG. 7.29. Determination of required dominant lag. Note that the open loop bandwidth has been drastically reduced by increasing the shunt capacitance of the pentode stage from 20 pF to 0·01 $\mu$F.

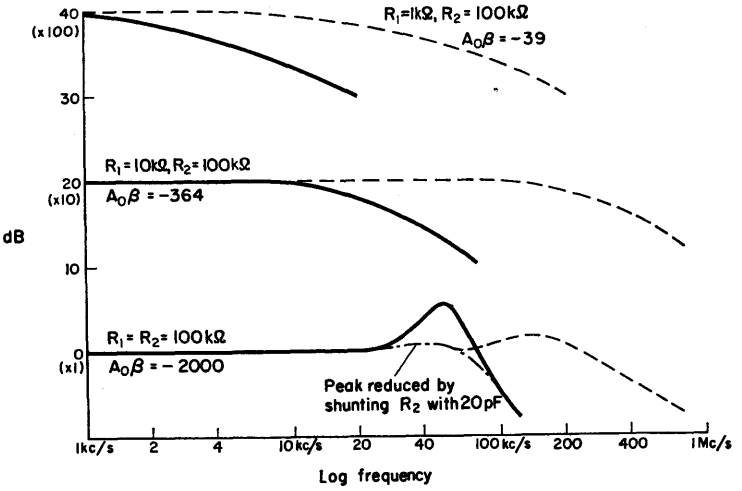



FIG. 7.30. Closed loop frequency response for (a) dominant lag stabilization (solid line) and (b) transitional lag stabilization. The $A$ gain is measured as $-4000$. The open loop bandwidth in the transitional lag case is 500 c/s and is 40 c/s in the dominant lag case.

Thus,

$$C_d = \frac{1}{2\pi f_1 R} = \frac{10^{-6}}{2 \times 20 \times 0{\cdot}8} \doteqdot 0{\cdot}01\ \mu\text{F}.$$

The closed loop performance obtained is shown in Fig. 7.30.

*Transitional Lag Stabilization*

This is a method that does not reduce the open loop bandwidth to the same degree as does dominant lag stabilization. Consider the network of Fig. 7.31 and its high and low frequency approximations.

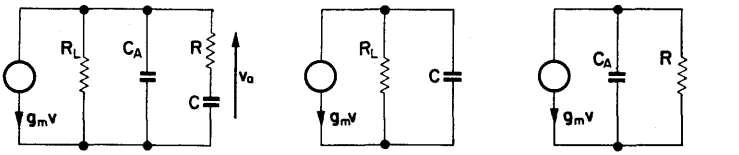



FIG. 7.31. Anode lag network with $C$ and $R$ added.

The impedance of the network for Fig. 7.31a is

$$Z(s) = R_L \frac{1 + sCR}{1 + s(CR + C_A R_L + CR_L) + s^2 CRC_A R_L} \tag{7.23}$$

$$\doteqdot R_L \frac{1 + sCR}{1 + sCR_L} \tag{7.24}$$

(if $C \gg C_a$ and $R \ll R_L$ and if the frequencies considered are below $\omega = 1/C_A R$).

The output voltage,

$$v_{\text{out}}(s) = -g_m R_L \frac{1 + sCR}{1 + sCR_L} v_{\text{in}}(s), \tag{7.25}$$

or

$$A(s) = A_0 \frac{1 + sCR}{1 + sCR_L} \tag{7.26}$$

(where $A_0 = -g_m R_L$).

If this network is combined with another which involves a simple lag, the latter can be made to cancel with the numerator of the above expression.

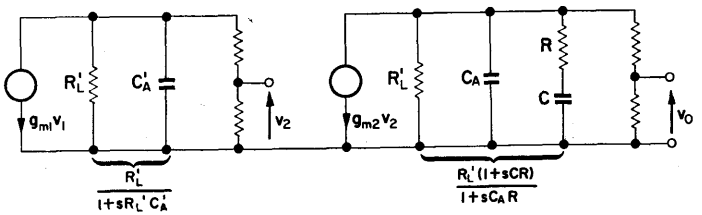



FIG. 7.32. Two-stage amplifier with second stage modified by the series $C$–$R$ circuit.

As shown in Fig. 7.32 the transfer function of the two-stage amplifier can be written as

$$A(s) = A_0' \frac{1 + sT}{(1 + sT_2)(1 + sT_1')}, \tag{7.27}$$

where $T = CR$, $T_1' = CR_L'$, $T_2 = C_A'R_L'$ and $A_0'$ equals the over-all gain at zero frequency.

If

$$T = T_2$$

then

$$A(s) = \frac{A_0'}{1 + sT_1'}. \tag{7.28}$$

The two-stage amplifier has been reduced from a two-lag system to a single lag, although there will be another lag at h.f. produced by the network shown in Fig. 7.31c.

The price paid for the controlled attenuation is a reduction in open loop bandwidth. If the stage with the lowest $f_1$ is the modified stage, the open loop bandwidth will fall from

$$\omega_1 = \frac{1}{C_A R_L} \quad \text{to} \quad \omega_1' = \frac{1}{CR_L}$$

and since $C \gg C_A$ the reduction will be considerable.

DESIGN EXAMPLE 7.2

Required, to stabilize the amplifier of Design Example 6.4 using a transitional lag.

It is required that the second breakpoint should lie on the unity gain line. In Fig. 7.33 a line is projected back from the intercept of the open loop gain asymptote and the unity gain

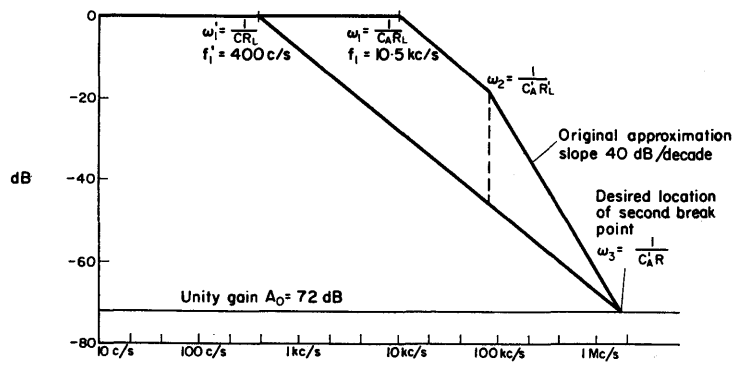



FIG. 7.33. Determination of transitional lag network. (a) Locate position of required breakpoint on original asymptote. (b) Project back at 20 dB/decade to find $\omega_1$. (c) Calculate $C = 1/(\omega_1 R)$ and $R = 1/(\omega_2 C)$.

line, at a slope of 20 dB/decade. The interception with the 0 dB relative gain axis is at $f_1' = 500$ c/s, so $\omega_1' = 3140$ r/s $= 1/CR_L$. Thus,

$$C = \frac{1}{R_L \omega_1'} = \frac{1}{0{\cdot}8 \times 10^6 \times 3{\cdot}14 \times 10^3} = 400 \text{ pF}.$$

For the cancellation of $(1 + sT)$ with $(1 + sT_2)$ it is required that $T = T_2$:

$$T_2 = \frac{1}{2\pi f_2} = 2{\cdot}13\ \mu\text{sec}.$$

Thus,

$$R = \frac{T}{C} = \frac{T_2}{C} = \frac{2{\cdot}13 \times 10^{-6}}{400 \times 10^{-12}} = 5{\cdot}3\ \text{k}\Omega.$$

The values for $C$ and $R$ can be checked by finding $f_3 = 1/2\pi C_A R$ which coincides with the point of intersection on the unity gain line.

## 7.9. The Drift Problem in Feedback Amplifiers

It has been mentioned in § 6.1 that although a d.c. amplifier has been zeroed, after a certain time, an output signal will be developed even though the input signal is zero. This is the drift signal.

Let the drift signal produced by an amplifier after a specified time be $v_{do}$. If feedback is applied, this quantity will be reduced to some value $v_{\text{out}}$. This implies a signal at the summing point $\beta v_{\text{out}}$, as in Fig. 7.34.

Thus the output voltage, due to drift,

$$v_{\text{out}} = v_{do} + A\beta v_{\text{out}} = \frac{v_{do}}{1 - A\beta} \tag{7.29}$$

$$\doteq -\frac{v_{do}}{A\beta} \quad (\text{if } A\beta \gg 1),$$

or

$$v_{\text{out}} = \frac{v_{di}}{\beta}, \tag{7.30}$$

where $v_{di}$ is the input referred drift voltage, i.e. $v_{di} = v_{do}/A_o$.

Thus the output drift is the equivalent input drift signal divided by the feedback fraction $\beta$. If $R_1 = R_2$, $\beta = \frac{1}{2}$ and for $v_{di} = 100$ mV, $v_{\text{out}} = 200$ mV.

The voltage $v_{di}$ is fictitious and does not exist physically at the input of the amplifier since, by definition, the input terminals are short circuited (see § 6.1). However, with feedback applied, there is a voltage $\beta v_{out}$ at the summing point and from the above equation this is $v_{di}$ which can be measured. This signal, when

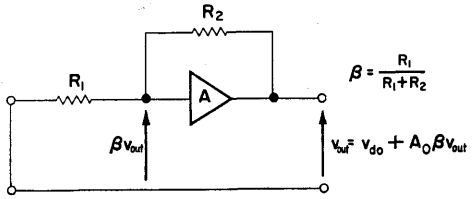



FIG. 7.34. Relationship between output drift voltage and voltage at the summing point.

amplified, opposes the output drift signal and, if $A\beta$ is large enough, almost cancels it. It should be noted that the gain is reduced to $G = \alpha A/(1 - A\beta)$ while the drift voltage is reduced to $v_{do}/(1 - A\beta)$. The drift voltage to signal ratio will be worsened by the factor $\alpha$ for an amplifier with feedback.

*Automatic Drift Correction*

The drift signal will give rise to error in a zero frequency amplifier system, unless the amplifiers are frequently zeroed. This would be tedious in a large computer. Some means of reducing the drift signal is thus desirable.

From eqn. (7.22), the output drift voltage $v_{out} = v_{do}/(1 - A\beta)$, where $v_{do}$ is the drift voltage of the amplifier without feedback.

Assuming that $v_{do}$ has been made as small as possible, and that $\beta$ is fixed by the feedback configuration, the only way of reducing $v_{out}$ is by increasing $A$. If $A$ is increased by an extra stage of amplification, $v_{do}$ will also be increased in proportion and the drift voltage will be approximately the same.

If the main amplifier, such as the three-valve d.c. amplifier previously considered, is preceded by an extremely low drift

amplifier which adds negligible drift, $v_{out}$ is reduced in the same proportion as $A$ is increased (see Fig. 7.35).

An amplifier with very low drift is the modulator type described in § 6.1. Such an amplifier has, however, a very narrow

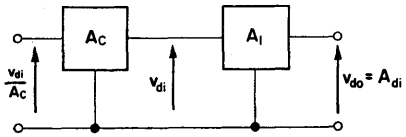



FIG. 7.35. Reduction of effective input-referred-drift by the addition of a driftless pre-amplifier.

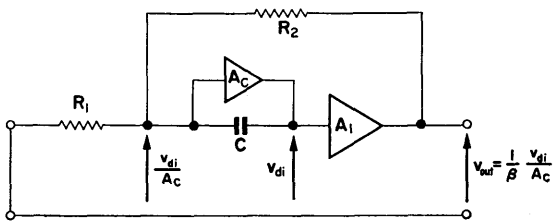



FIG. 7.36. Use of auxiliary amplifier to provide automatic zeroing. Drift voltage of $A_1$ is reduced by the gain of $A_c$.

bandwidth and is quite inadequate for high speed computing. It can be bypassed for high frequency signals by a capacitor as in Fig. 7.36, thereby providing a gain, at computing frequencies, of $A_1$.

The zero frequency gain $A_0 = A_c A_1$.

$$\text{Equivalent input drift} = \frac{v_{di}}{A_c}.$$

$$\text{Output drift} = \frac{1}{\beta}\frac{v_{di}}{A_c} = 2 \times \frac{100\text{ mV}}{1000} = 200\ \mu\text{V}.$$

$$(\text{for } v_{di} = 100\text{ mV and } A_c = 1000)$$

The capacitor $C$ may be undesirable in some applications as, in conditions of overload, it can be charged by grid current. Because of the normally high input impedance to $A_1$, the discharge time can be excessive. With valve systems, the grid of the

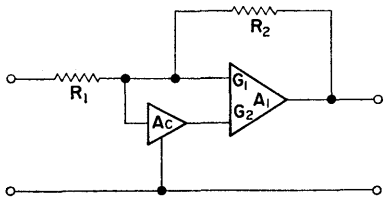



FIG. 7.37. Auxiliary amplifier connection for main amplifier with longtail pair dual input. The auxiliary amplifier has signal inversion.

second valve of the longtail pair can be used as the input from the auxiliary amplifier.

Referring to Fig. 7.37 the zero frequency gain $= A_1 + A_1A_c = A_1(1 + A_c)$.

If the drift of the main amplifier is $v_{dI}$, and the auxiliary amplifier drift is negligible, the output drift with feedback,

$$v_{\text{out}} = \frac{v_{do}}{A_o\beta} = \frac{1}{\beta}\left[\frac{v_{di}A_1}{A_1(1 + A_c)}\right] = \frac{1}{\beta}\left[\frac{v_{di}}{1 + A_c}\right].$$

## 7.10. A SHUNT–SHUNT AMPLIFIER WITH DEFINED TRANSFER RESISTANCE

### DESIGN EXAMPLE 7.3

Required, a d.c. amplifier with a transfer resistance of $-100\,\text{k}\Omega$ and output voltage swing $\pm 5$ V.

The three-stage amplifier of Design Example 6.4 has an internal transfer resistance of $-60\,\text{M}\Omega$. The required overall transfer resistance is $-100\,\text{k}\Omega$. $R_T = \dfrac{-R_F}{1 + (R_F/Z_t)}$.

The loop gain is

$$\frac{Z_t}{R_F} = -\frac{60 \times 10^6}{100 \times 10^3} = -600.$$

Thus the overall transfer resistance is defined to an error of

$$\frac{R_F}{Z_t} . 100\% = 0{\cdot}16\% \quad \text{(see § 7.2e)}.$$

The phase shift provided by the three stages will be sufficient to produce oscillation and some form of stabilization is necessary. A very convenient method is to provide a lag by increasing the "Miller" capacitance of one of the transistors. This has the advantage of requiring a relatively small capacitor.

*Method of stabilization.* As shown in Fig. 7.38, insert a sufficiently large capacitor between collector and base of the first stage to stop oscillation. This will be of the order of 0·1 μF. Now reduce its value in steps until a value is found that ensures stability without an excessive reduction of bandwidth. The band-

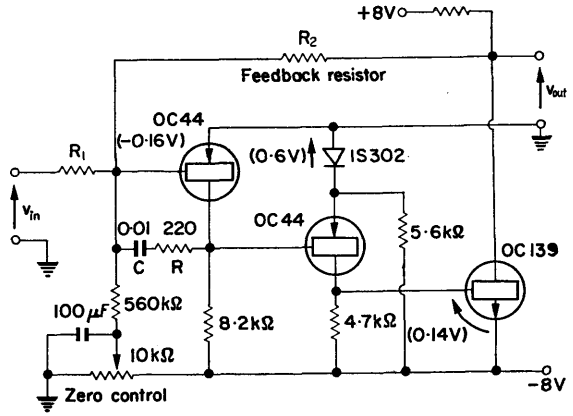



FIG. 7.38. D.C. amplifier with transfer resistance $R_T = 100\,\text{k}\Omega$, and internal transfer impedance of $-60\,\text{M}\Omega$. $C$ and $R$ are stabilization elements.

width can be further extended by inserting resistance in series with the capacitor. This should be of the order of 10 Ω to begin with, and be increased until a satisfactory compromise between stability and bandwidth is obtained. With this amplifier $R = 220\,\Omega$ and $C = 0{\cdot}01\ \mu F$ are suitable values, and its performance under various conditions of feedback is shown in Fig. 7.39.

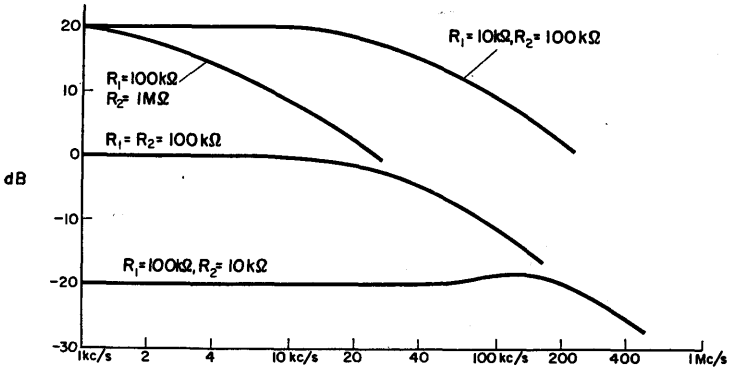



FIG. 7.39. Amplitude-frequency response of an amplifier with internal transfer impedance of −60 MΩ. Bandwidth is a function of $R_2$ and is independent of gain. The two curves for $R_2 = R_T = 100$ kΩ show the same bandwidth, although one is for 10 times the gain of the other.

## 7.11. CURRENT AMPLIFIER WITH DEFINED GAIN

Such an amplifier has been described in § 7.2 (type b).

### DESIGN EXAMPLE 7.4

Required, a d.c. amplifier with current gain of 100, nominal input resistance 100 Ω and providing an output current of 2 mA into a 4 kΩ load.

With such an amplifier the requirement is to make the performance largely independent of the transistor parameters, principally the current gain $h_{fe}$. This requires the loop gain

$|A_0\beta|$ to be much greater than unity. Then the gain,

$$G = \frac{A}{1 - A_0\beta} \doteqdot \frac{1}{\beta}.$$

*Transistors.* General purpose alloy type OC44 transistors are suitable.

*Power supply.* The maximum voltage to be developed across $R_L$ is

$$V_{L(\max)} = 2\text{ mA} \times 4\text{ k}\Omega = 8\text{ V}.$$

A 10 V supply will be satisfactory as it allows a minimum of 2 V across $R_2$ and $T_2$, in Fig. 7.40.

*Feedback resistors $R_1$ and $R_2$.* For $|A_0\beta| \gg 1$ the gain of the amplifier is $1/\beta$, where $\beta = R_2/(R_1 + R_2)$, i.e. the fraction of the output current fed back to the input.

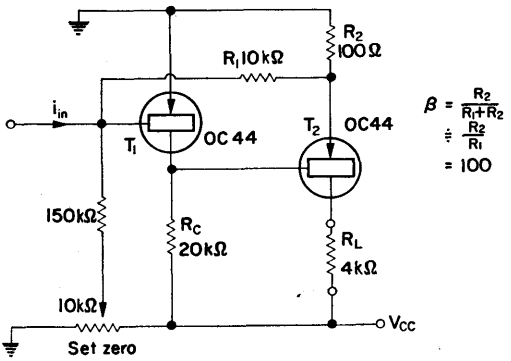



FIG. 7.40. Current amplifier with current gain defined by $R_1/R_2$.

*Input resistance.* This is approximately $r_{in} = R_b/(1 - A_0\beta)$ where $R_b$ is the input resistance to the $A$ amplifier without feedback.

*Collector resistor* $R_C$. $T_1$ is run at 0·5 mA, and for a 10 V supply,

$$R_C = \frac{V_{CC}}{I_C} = \frac{10\text{ V}}{0{\cdot}5\text{ mA}} = 20\text{ k}\Omega.$$

*Estimation of* $R_b$ *of* $T_1$. The value of the short circuit current gain of $T_1$ is estimated, from the collector characteristic, as 60 under the selected operating conditions.

$$\text{Input resistance of } T_1,\ R_{b1} \doteqdot h_f R_e.$$

The forward characteristic of the junction as shown in Fig. 2.1 b can be expressed as

$$I = I_{co} \quad \exp\left(-\frac{eV}{kt}\right)$$

from which

$$\frac{\mathrm{d}I}{\mathrm{d}V} = I \Big/ \left(\frac{kT}{e}\right).$$

But the forward resistance $R_e = \mathrm{d}V/\mathrm{d}I$ where $V$ is the forward voltage. Therefore

$$R_e = \left(\frac{kT}{e}\right) I.$$

At normal temperature $kT/e = 25$ mV. Therefore

$$R_e = \frac{25}{I_E(\text{mA})} = 60 \times 50 = 3\text{ k}\Omega.$$

*Estimation of* $R_b$ *of* $T_2$. $R_{b2} \doteqdot h_f(R_2 + R_e)$, where $R_e = 25/(1{\cdot}25\text{ mA}) = 20\,\Omega$, and, $I_E$ is for $V_{C2} = -5$ V. The short circuit current gain, $h_f$ from the collector characteristics under the selected operating conditions, is 90.

Therefore

$$R_{b2} = 11\text{ k}\Omega.$$

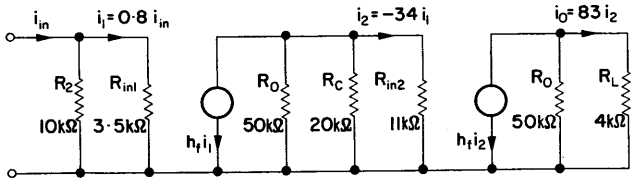



FIG. 7.41. Equivalent network for estimation of $A$ gain. $R_2$ is taken to the common line to eliminate feedback.

*A gain.* From the equivalent network of Fig. 7.41 the estimated current gain,

$$\frac{i_{out}}{i_{in}} = 2260,$$

thus the loop gain for $\beta = 100$,

$$A_0\beta \doteqdot -23.$$

Also, the input resistance, with feedback,

$$R'_{in} = \frac{3\ \text{k}\Omega}{1 + 23} = 125\,\Omega.$$

The open and closed loop amplitude response for the amplifier is shown in Fig. 7.42.

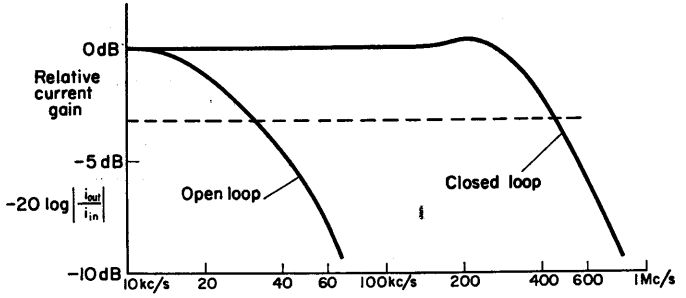



FIG. 7.42. Open and closed loop amplitude response for the feedback current amplifier. Nominal loop gain $A_0\beta = -23$.

CHAPTER 8

# Power Supplies

## Introduction

The most convenient source of power to operate electronic equipment is the supply mains. This has the advantage of cheapness and constancy, when compared with batteries, but a disadvantage is the inevitable introduction of mains frequency noise. The conversion from a.c. to unidirectional current can be most efficiently carried out by semiconductor diodes. These have low forward resistance, require no auxiliary power and can be used in applications where it would be difficult to supply the heater power to thermionic valves.

## 8.1. The Basic Rectifier

In the circuit of Fig. 8.1 the diode conducts on alternate half-cycles and the average (or d.c.) value of output voltage is $V_R/\pi$.

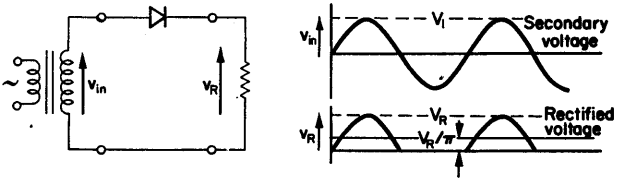



FIG. 8.1. The half wave rectifier.

The voltage applied across the diode during negative half-cycles is known as the inverse voltage, and if this exceeds the inverse voltage rating of the component, breakdown may occur. The

maximum inverse voltage rating varies from a few volts for small components to several thousand volts for high voltage diodes.

## 8.2. Full Wave Rectifier

To increase the average value of the output voltage from $V_R/\pi$ to $2V_R/\pi$ two diodes can be used in a full wave system. One diode conducts on the positive half-cycle of alternating

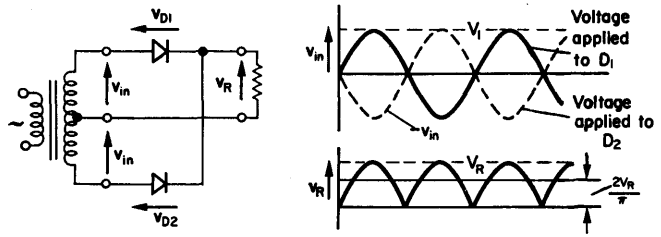



FIG. 8.2. The full wave rectifier.

voltage, and the other during the negative half-cycle. Such an arrangement, shown in Fig. 8.2, requires a transformer having a centre tapped secondary winding.

Full wave rectification may also be obtained without a centre tapped secondary by making use of the bridge circuit of Fig. 8.3.

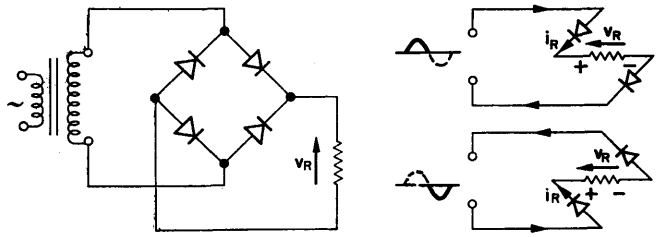



FIG. 8.3. The bridge rectifier. The manner in which pairs of diodes operate during alternate half-cycles is illustrated.

While thermionic diodes cannot be conveniently used in this configuration, semiconductor diodes, because of their small physical size and no heater requirements, are eminently suitable.

## 8.3. Effect of Load Capacitance

Referring to Fig. 8.4, the load capacitor charges when $v_{in}$ is greater than $v_R$ and during the remainder of the cycle supplies the load current $i_L$. If the time constant $CR$ is much greater than the

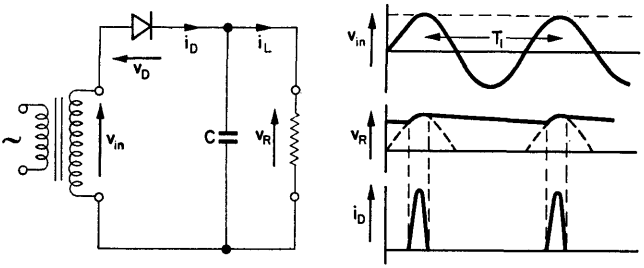



FIG. 8.4. Effect of reservoir capacitor on the output of a rectifier circuit.

period $T_1$, the output voltage will not change appreciably over the period. It should be noted that the peak current passed by the diode can be many times the load current.

### *Output Ripple*

The output voltage changes during the period and this change constitutes the ripple output. Provided that the $CR$ time constant is much greater than the period $T_1 = 1/f$, and consequently diode current only flows for a short time, the ripple approximates to a sawtooth waveform as shown in Fig. 8.5.

The change in charge on the capacitor,

$$\Delta Q = \Delta VC = I_L T_1,$$

where $I_L$ is the average load current.

Thus,

$$\Delta V = \frac{I_L T_1}{C} = \frac{V_{av} T_1}{CR} \quad (\text{since } I_L = V_{av}/R). \tag{8.1}$$

The average value of output voltage,

$$V_{av} = V_1 - \frac{V_{av} T_1}{2RC} \doteqdot V_1 \left(1 - \frac{T_1}{2RC}\right) \quad (\text{since } V_{av} \doteqdot V_1).$$

Therefore

$$V_{av} = V_1 \left(1 - \frac{1}{2fRC}\right). \tag{8.2}$$

For full wave rectification the ripple frequency is twice the

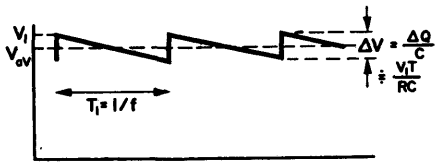



FIG. 8.5. Output ripple. Provided that the $CR$ time constant is much greater than $T = 1/f$, output ripple approximates to a sawtooth waveform.

mains frequency, i.e. $T_2 = 1/2f$. In this case the peak to peak ripple voltage,

$$\Delta V = \frac{V_1}{2fRC}. \tag{8.3}$$

EXAMPLE. A full wave rectifier supplied from a mains source of $f = 50$ c/s and having a peak value $V_1 = 100$ V. If $C = 100\,\mu$F and the load current $I_L = 10$ mA,

$$\Delta V = \frac{V_1}{2fRC} = \frac{100}{2 \times 50 \times 10^4 \times 10^{-4}} = 1 \text{ V}.$$

$$\text{Percentage ripple} = \Delta V / V_1 \times 100 = 1\%.$$

*Output filter for ripple reduction.* The ripple voltage may be reduced by using a low pass filter which, in its simplest form, is the series resistor and shunt capacitor of Fig. 8.6. This is a voltage dividing network in which the output ripple is developed across the capacitor, which is selected to have a much lower impedance than $R$.

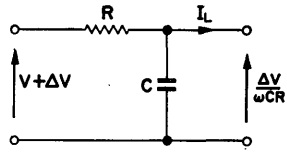



FIG. 8.6. Output filter for reduction of ripple. Ripple reduction factor $\gamma = 1/\omega CR$.

A disadvantage of the system is that the load current flows through $R$, increasing the power supply resistance. The output voltage will therefore fall as the load current is increased. For $R$–$C$ smoothing, the ripple reduction factor,

$$\gamma = 1/\omega CR. \tag{8.4}$$

## 8.4. $L$–$C$ SMOOTHING FILTER

If an inductance is used in place of the resistance, as in Fig. 8.7, two advantages result. Firstly, the d.c. voltage drop is greatly reduced because of the low resistance of the choke. Secondly,

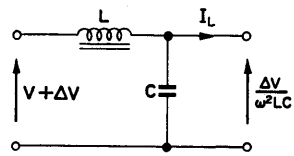



FIG. 8.7. $L$–$C$ smoothing filter. Ripple reduction factor, $\gamma = 1/\omega^2 LC$.

the impedance of the choke is proportional to frequency. Thus, the output ripple is reduced from $\Delta V$ to $\Delta V/\omega_r^2 LC$, where $\omega_r$ is $2\pi$ times the ripple frequency.

For $L$–$C$ smoothing, the ripple reduction factor,

$$\gamma = 1/\omega_r^2 LC. \tag{8.5}$$

Referring to the previous example, if the percentage ripple is to be reduced from 1 to 0·1 %,

$$\omega_r^2 LC = 10, \quad \text{or} \quad L = 10/\omega_r^2 C.$$

Thus, for a ripple frequency of 100 c/s and $C = 10\ \mu\text{F}$, $L = 2{\cdot}5\ \text{H}$.

## 8.5. Choke Input Filter

When the filter of Fig. 8.7 is used directly with the full wave rectifier of Fig. 8.2 the power supply is known as a choke (or inductance) input type. The filter selects the average component of the rectifier output but removes the ripple.

From Fourier analysis, the series expression for the rectifier output voltage is

$$v = \frac{4V_1}{\pi}\left[\frac{1}{2} + \frac{\cos 2\omega t}{3} - \frac{\cos 4\omega t}{15} + \cdots\right], \tag{8.6}$$

where $\omega = 2\pi$ times the supply frequency.

The average, or d.c. component, is $2v_1/\pi = 0{\cdot}64\ V_1$.

The lowest frequency ripple component has an amplitude of $4V_1/3\pi$ and is twice the supply frequency. This is the major component of the ripple.

The load current,

$$I_R = \frac{V_R}{R} = \frac{2V_1}{\pi R}. \tag{8.7}$$

If it is assumed that the capacitor has a very low impedance at the ripple frequency, the principal ripple component,

$$I_c = \frac{4}{3}\frac{V_1}{\pi}\frac{1}{2\omega L}. \tag{8.8}$$

This analysis is only valid if the load current $I_R$ is always greater

than $i_c$ so that one or other of the rectifiers is conducting at all times, producing the current and voltage waveforms of Fig. 8.8.

$$\text{Output ripple voltage} = \frac{I_c}{2\omega C} = \frac{V_1}{3\pi\omega^2 LC} \quad \text{[from eqn. (8.8)]}$$

$$\doteqdot \frac{0{\cdot}1V_1}{\omega^2 LC}. \tag{8.9}$$

The ripple is thus independent of the load current which is not the case when a reservoir capacitor is used.

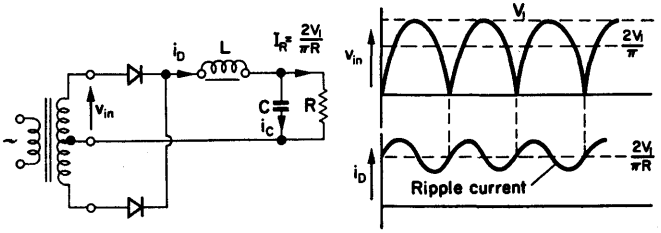



FIG. 8.8. Full wave rectifier with choke input filter. Provides good regulation, low rectifier peak currents but relatively low output voltages.

EXAMPLE. For, $\omega = 2\pi 50$ r/s, $L = 2{\cdot}5$ H, $C = 100$ μF and $V_1 = 100$ V, the output ripple voltage is 0·8 V peak-to-peak. The minimum current for correct operation is $I_R \geqslant I_C$. Thus, to determine the maximum value of $R$, equate eqns. (8.7) and (8.8),

$$\frac{2V_1}{\pi R} = \frac{4}{3}\frac{V_1}{\pi}\frac{1}{2\omega L},$$

from which, $R = 3\omega L = 2{\cdot}4$ kΩ. If $R$ is more than this value, the inductor is unable to store sufficient energy to ensure that one rectifier is conducting at all times.

In general, choke input filters have good voltage regulation and low rectifier peak currents but give relatively low output voltages. The use of a reservoir capacitor, as in Fig. 8.9, provides

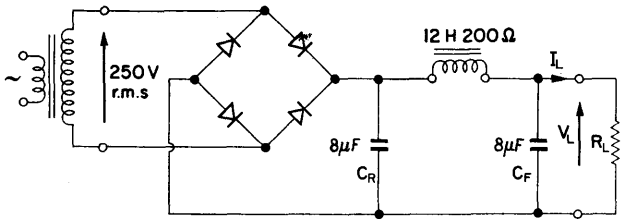



FIG. 8.9. Full wave rectifier with capacitor input filter. Provides high output voltages, but has high rectifier peak currents and relatively poor regulation.

a capacitor input filter, which has high output voltages but poor regulation and high rectifier peak currents. Capacitor input filters are used where the load is relatively constant as, for instance, in radio receivers. Comparison of the two types of filter circuits is made in the graph of Fig. 8.10.

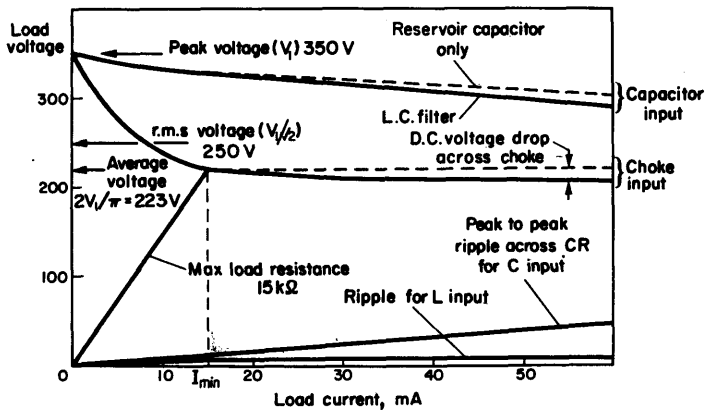



FIG. 8.10. Comparison of the performance of the two types of output filter circuits. The output voltage is the same for both systems, under zero load conditions, but in the case of the choke input filter it falls rapidly until the effective load resistance is 15 kΩ. Thereafter it remains constant.

## 8.6. VOLTAGE MULTIPLIERS

Two rectifiers of the type shown in Fig. 8.4 may be used with the same transformer winding. If the diodes are connected in opposite manner, as in Fig. 8.11, the two d.c. outputs are

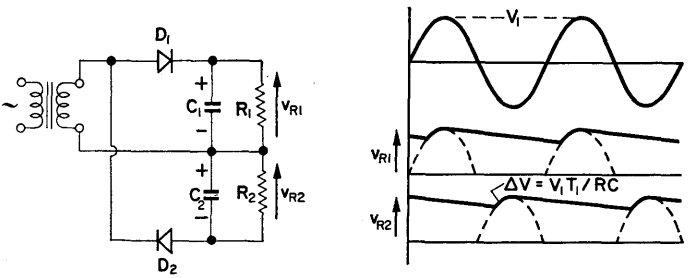



FIG. 8.11. The voltage doubler. If the load current is small, the output voltage is twice the peak value of input voltage.

effectively added giving an output voltage approaching twice the peak input voltage.

An alternative form of voltage multiplier is given in Fig. 8.12. This has a common connection between input and output, which

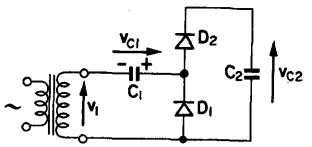



FIG. 8.12. Alternative form of voltage doubler.

can be a desirable feature in some applications. On negative half-cycles of $V_1$, $C_1$ charges up to the peak value of $V_1$ through $D_1$. On positive half-cycles $D_1$ is non-conducting and the anode of $D_2$ is raised to twice the peak value of $V_1$. After a number of cycles $C_2$ charges to $2V_1$.

Any number of stages may be employed in this circuit arrangement, enabling very large voltages to be developed from low volt-

age sources. In Fig. 8.13, $C_3$ will charge to $V_{C2}$ through $D_3$ and then will be raised $2V_1$ by the charge on $C_1$. The voltage across $C_3$ will charge $C_4$ through $D_4$. Similarly, $C_5$ will charge to the voltage across $C_4$ through $D_5$ and then be raised $2V_1$ by $C_3$. Each of the output capacitors is charged to $2V_1$ thus providing an output voltage 6 times the peak input voltage.

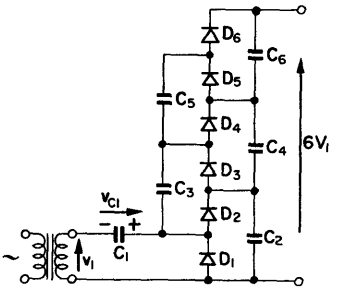



FIG. 8.13. The voltage multiplier. The circuit is a development of Fig. 8.12 and may be extended to provide very large voltages.

## 8.7. VOLTAGE STABILIZATION

The power supplies so far described have output voltages determined by two main factors: (a) the supply voltage, and (b) the load current drawn. Changes in either of these will cause the output voltage to change. In order to make the output voltage relatively insensitive to variations in supply voltage, or load current, some form of voltage stabilization is necessary.

### *Gas Discharge Tube*

A simple way of ensuring that the output voltage is stable is to use the constant voltage developed across a gas discharge, as in Fig. 8.14.

### DESIGN EXAMPLE 8.1

Required, a nominal 100 V supply for a 25 mA load current derived from a 200 V source.

A suitable discharge tube is the 108 C1 (the 108 indicates the operating voltage), having an operating current range of 5–30 mA and requiring a striking voltage of 140 V.

In order to accommodate changes in load current it is desirable to operate the tube near the middle of its current range. Let $I_N$ be 20 mA. From Fig. 8.14, the input current, $I = I_N + I_L = 20 + 25 = 45$ mA.

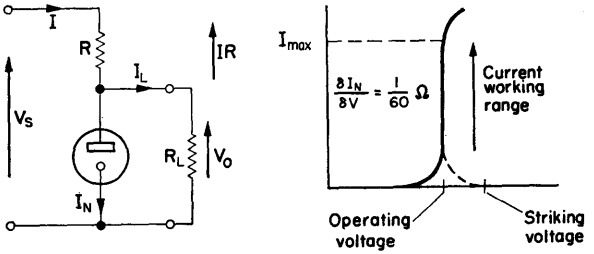



FIG. 8.14. Use of a gas discharge tube to provide voltage stabilization.

The value of the series resistor $R$, necessary to drop the voltage from $V_S$ to $V_O$ is given by:

$$R = \frac{V_S - V_O}{I_N + I_L} = \frac{92\text{V}}{45\text{ mA}} \doteqdot 2\text{ k}\Omega.$$

As $I_L$ is reduced the current through the tube increases. Thus the load current can vary from 25 to 40 mA without an appreciable change in the output voltage.

*Differential resistance.* This is the change in tube voltage for a given change in tube current and is of the order of 100 Ω. Thus a change of 5 mA will change the output voltage by approximately 0·5 V.

*Striking voltage.* As shown in Fig. 8.14, a higher voltage than the operating voltage is required to initiate the discharge, and $V_S$ must be sufficient for this purpose. Some discharge tubes have

an auxiliary trigger electrode which is used for striking the discharge.

The range of discharge tube stabilizers is from 50 to 150 V, but higher voltages can be stabilized by using two tubes in series. In this case provision must be made for striking one tube independently of the other. A method is shown in Fig. 8.15 in

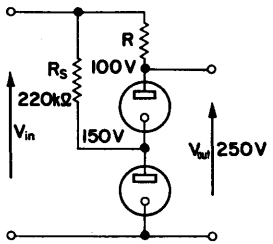



FIG. 8.15. Voltage stabilization using two gas discharge tubes in series. The resistor $R_s$ provides a path for striking the lower regulator.

which $R_S$ provides a path for striking the lower regulator. The upper tube strikes subsequently due to the source voltage.

*Voltage reference tubes.* The discharge tube, by operating at a specified current, gives a defined voltage that can be used as a reference voltage source. Special tubes are available for this purpose and a common reference voltage is 85 V. (See Design Example 8.5.)

*High voltage stabilizers.* The corona discharge at high voltage can be used to stabilize voltages of the order of 1000 V. Operation is in a manner similar to that described for gas discharge tubes but operating current levels are much lower.

## 8.8. SEMICONDUCTOR STABILIZER DIODES

Junction diodes can be produced with a well-defined breakdown voltage when operated with reverse voltage applied. A typical characteristic for a silicon breakdown diode is given in

Fig. 8.16. The usual range of operation is from 3 to 20 V. The manner of application is similar to that of gas discharge tubes but no striking voltage is required. Large currents can be passed by breakdown diodes but, since the device maintains a constant voltage across itself, the maximum safe current is determined by the power dissipation of the device. This is from 200 mW for a small free mounted device to several watts for a stud mounted diode.

The breakdown voltage is a function of temperature with a typical variation of from $-2$ to $+8$ mV/°C. Diodes with temperature coefficients of the order of 10 $\mu$V/°C can be obtained for use as voltage reference sources. When used for this purpose the diode should be operated from a constant current supply.

DESIGN EXAMPLE 8.2

Required, from a 20 V source, a stabilized voltage supply having a nominal voltage of 6·8 V and providing a load current of 15 mA $\pm$ 10 mA.

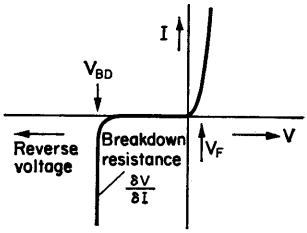



FIG. 8.16. Typical characteristic of a silicon breakdown diode.

The circuit arrangement is as shown in Fig. 8.17a while in Fig. 8.17b is drawn an approximation of the supply output.

A 1S7068A diode has a nominal breakdown voltage of 6·8 V and an incremental resistance, $\delta V/\delta I = 2\ \Omega$ at a current of 15 mA.

The maximum load current will flow when the diode current is a minimum. If the minimum diode current is 15 mA, then the current drawn from the source is

$$I = I_L + I_D = 25\text{ mA} + 15\text{ mA} = 40\text{ mA}.$$

The voltage to be dropped across the series resistor is

$$V_R = V_S - V_{BD} = 20\text{ V} - 6{\cdot}8\text{ V} = 13{\cdot}2\text{ V}.$$

$$R_S = \frac{V_R}{I} = \frac{13{\cdot}2\text{ V}}{40\text{ mA}} = 330\,\Omega.$$

The output voltage falls approximately $\Delta V_L = R_{out}\Delta I_L$ as the load current increases from its minimum to its maximum value.

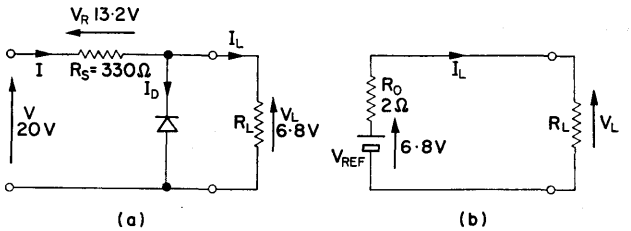



FIG. 8.17.(a) Circuit arrangement of Design Example 8.2, with (b) an approximate representation of the supply output.

Thus, $\Delta V_L = 2 \times 20 \times 10^{-3} = 0{\cdot}04$ V.

Under these conditions the maximum possible dissipation in the diode is $IV_L \doteqdot 300$ mW, which is well within the stated dissipation of the device.

## 8.9. CATHODE FOLLOWER AS VOLTAGE STABILIZER

It was shown in Fig. 1.24 that the output voltage of a cathode follower closely follows the grid voltage. If the grid voltage is held at some constant value, the cathode will be at nearly the same value, and largely independent of the current through, or the voltage across, the valve.

A circuit diagram of a cathode follower voltage stabilizer is given in Fig. 8.18a, in which $R$, the unregulated supply resistance, will normally be less than the $r_a$ of the valve. In the equivalent network of the output (Fig. 8.18b), $R_{out}$ is the effective incremental resistance.

The output voltage,

$$V_O = V_G - V_{GK}, \tag{8.10}$$

where $V_{GK}$ is the grid–cathode voltage necessary to provide the load current. Change in output voltage, as the load is varied, is due to the change in $V_{GK}$ necessary to maintain the current. For instance, with $\mu = 50$ and $r_a = 10\ \text{k}\Omega$, a change of 10 mA

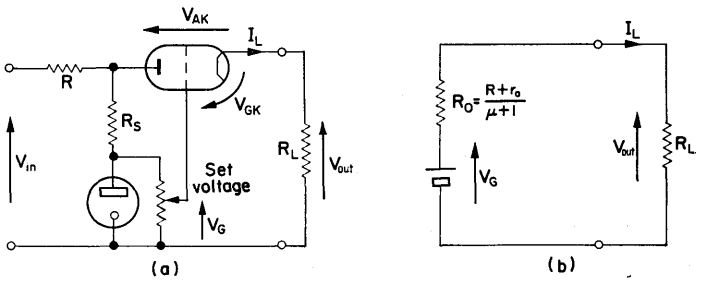



FIG. 8.18. The cathode follower voltage stabilizer and its equivalent output network.

in load current will cause an output voltage change of approximately 2 V. For this application a valve with a high $g_m$ is desirable.

DESIGN EXAMPLE 8.3

Required, a stabilized 150 V supply to provide a maximum load current of 75 mA.

*Series valve.* Referring to Fig. 8.18a, $V_{AK}$ is the difference between the unregulated and regulated voltages. The series valve passes the load current $I_L$, and has this excess voltage dropped across it. It must therefore be capable of dissipating the power $V_{AK}I_L$ watts. Using the system of Fig. 8.9 with a choke input filter, the excess voltage will be about 65 V which, at a current of 75 mA, produces a power of approximately 5 W. Let the valve chosen be an A2293 triode having a maximum dissipation of 15 W, an $r_a$ of 700 Ω and a $\mu$ of 6. (Note the very low amplifica-

tion factor for this type of valve.) From the anode characteristics, plotted in Fig. 8.19a, it is apparent that, with an anode voltage of about 60 V, the required load current can be passed with $V_{GK}$ still several volts negative.

*Reference supply.* A 150 V stabilizer tube is used as the grid voltage reference, and operated at a nominal current of 10 mA. The resistor $R_g$ supplies the striking voltage, and its value is such that when carrying 10 mA it provides approximately 150 V to the stabilizer tube.

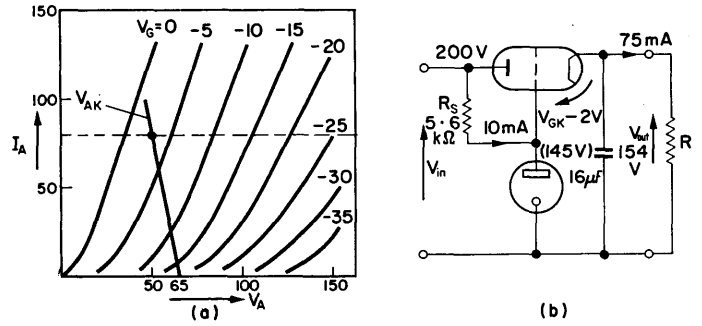



FIG. 8.19. Circuit diagram for Design Example 8.3, and the characteristics of the A2293 triode.

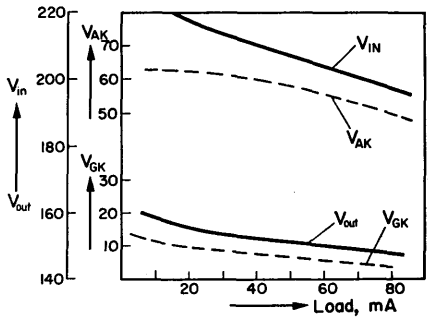



FIG. 8.20. Performance of the circuit of Design Example 8.3. Cathode follower voltages are plotted against load current.

The circuit diagram of the cathode follower stabilizer is given in Fig. 8.19b with conditions for an output current of 75 mA. The capacitor ensures a low supply impedance at high frequency.

*Performance.* In Fig. 8.20 the cathode follower voltages are plotted against load current. The source resistance, that is the resistance of the unstabilized supply, is given by the slope of $V_{IN}$ and is approximately 400 Ω. The output resistance can be obtained from the expression of Fig. 8.18b,

$$R_{out} = \frac{r_a + R}{\mu + 1} = \frac{700 + 400}{6 + 1} = 160\,\Omega.$$

## 8.10. Emitter Follower as Voltage Stabilizer

The output voltage from an emitter follower is the base voltage less the base–emitter voltage required to maintain the emitter current. Since $V_{BE}$ is usually small, the emitter voltage closely follows the base voltage and the system is comparable with the cathode follower stabilizer of the previous example. The load current is effectively the emitter current, which equals the base current times the current gain of the output transistor. The input current to the stabilizer can be reduced by using a compound emitter follower.

### Design Example 8.4

Required, a current variable over the range 10–60 mA at −10·5 V from a regulated −20 V supply.

The circuit diagram of a compound emitter follower stabilizer is given in Fig. 8.21.

*Current gain.* The current gain should be sufficient to ensure that the base current of the input transistor is negligible compared with the current drawn by the resistance chain. The latter is 1 mA and, for a current gain of 2000 the maximum base

current,

$$I_B = \frac{60 \text{ mA}}{2000} = 30 \ \mu\text{A}.$$

The change in voltage at the base of $T_1$, as the load current changes from minimum to maximum, will be approximately 0·25 V.

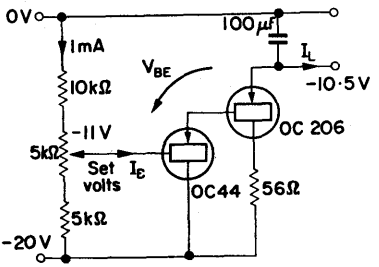



FIG. 8.21. Compound emitter follower stabilizing circuit of Design Example 8.4.

*Output transistor.* A current of 60 mA is required. An OC206 transistor is capable of passing such a current and its collector dissipation is 400 mW. However, with the full excess voltage of 9·5 V, and at the maximum load current, the dissipation is 570 mW. A resistor is therefore included in the collector circuit to reduce the voltage dropped across the transistor. In this case

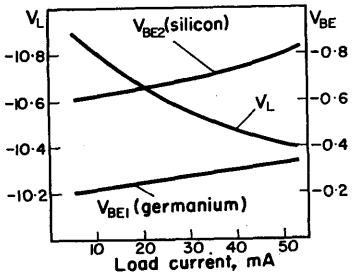



FIG. 8.22. Changes in $V_{BE}$ required to maintain the load current, plotted for the two transistors of Fig. 8.21. Total $V_{BE} = V_{BE1} + V_{BE2}$.

a 56 Ω resistor will reduce the maximum dissipation of the output transistor to 360 mW. This resistor also serves as protection for the transistor when excess load current is drawn.

*Output impedance.* An electrolytic capacitor across the output terminals ensures that the supply has low impedance at high frequency. At low frequency the high current gain ensures that the output impedance is low. The main change in output voltage, as the load current varies, is due to the change in $V_{BE}$ required to maintain the load current. This is illustrated in the graph of Fig. 8.22.

## 8.11. Closed Loop Voltage Regulator

The two previous stabilizers perform as simple closed loop systems. Referring to the cathode follower circuit (Fig. 8.18), as $I_L$ is increased $V_{GK}$ is increased (i.e. becomes less negative) to supply the demand, thus reducing the voltage across the valve and offsetting the increased voltage across $R$.

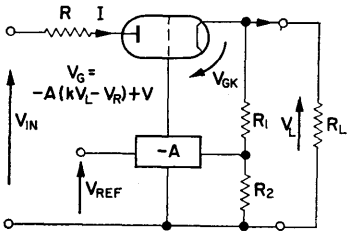



FIG. 8.23.
Closed loop voltage regulator. The symbol $k = R_2/R_1 + R_2$.

Since, from eqn. (8.10), $V_O = V_G - V_{GK}$, an increase in $V_{GK}$ will cause the output voltage to fall. This fall can be counteracted by increasing $V_G$. The output voltage $V_O$ is compared with a reference voltage and any change is inverted, amplified and fed to the grid. Such a system is illustrated in Fig. 8.23. The grid voltage,

$$V_G = -A(kV_L - V_R) + V, \qquad (8.11)$$

where $V$ is the voltage at the amplifier output when $kV_L = V_R$. The load voltage, $V_L = I_L R_L \doteqdot IR_L$ where $I$ is the current from the rectifier. From eqn. (8.10), $IR_L = V_G - V_{GK}$ and, substituting eqn. (8.11) for $V_G$,

$$IR_L = -A(kV_L - V_R) + V - V_{GK}$$

$$= -A(kIR_L - V_R) + V - V_{GK}.$$

Therefore

$$I(R_L + AkR_L) + AV_R = V - V_{GK},$$

or

$$IR_L = \frac{AV_R + V - V_{GK}}{(1 + Ak)}$$

and

$$V_L = \frac{V_R + [(V - V_{GK})/A]}{1/A + k}. \tag{8.12}$$

It is seen that changes in $V_{GK}$ are reduced by $1/A$.
If the gain $A$ is sufficiently large,

$$V_L = \frac{V_R}{k}. \tag{8.13}$$

The output voltage can be set by varying either $V_R$, the reference voltage, or $k$, the proportion of the output voltage applied to the difference amplifier.

*Incremental Representation*

The output resistance, ripple voltage and stabilization against input voltage changes can be determined from the incremental equivalent network of Fig. 8.24:

$$i \doteqdot \frac{v_{in} + \mu v_{gk}}{R_{in} + r_a + R_L}. \tag{8.14}$$

Since $R_1 + R_2$ is much greater than $R_L$, these resistors may be neglected:

$$i = \frac{v_{in} - \mu(Ak + 1)\, v_L}{R_{in} + r_a + R_L} = \frac{v_{in} - \mu(Ak + 1)\, iR_L}{R_{in} + r_a + R_L}, \quad (8.15)$$

from which,

$$i = \frac{v_{in}}{R_{in} + r_a + R_L + \mu R_L(Ak + 1)}.$$

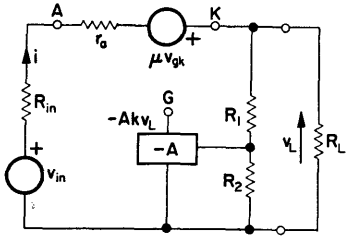



FIG. 8.24. Equivalent network of the closed loop voltage regulator, to investigate output resistance, ripple voltage and stabilization.

Therefore

$$v_L = iR_L = \frac{v_i R_L}{R_{in} + r_a + R_L[1 + \mu(Ak + 1)]}.$$

If $A$ is large,

$$v_L = \frac{[v_{in}/(1 + \mu Ak)]\, R_L}{[(R_1 + r_a)/(1 + \mu Ak)] + R_L}. \quad (8.16)$$

From this equation an equivalent circuit (Fig. 8.25) can be drawn as the incremental representation of the power supply.

DESIGN EXAMPLE 8.5

Required, a 150 V, 75 mA supply with nominal output resistance of 20 Ω. The ripple voltage must be less than 10 mV peak-to-peak at full load current.

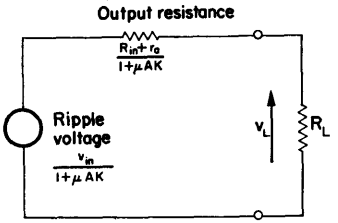



FIG. 8.25. Incremental representation of the closed loop voltage regulator output circuit.

To achieve the low output resistance a closed loop system is necessary and this takes the form of Fig. 8.26.

*Difference amplifier.* A cathode coupled amplifier is desirable for this purpose as it has inherent low drift.

Referring to Fig. 8.10, the output impedance of the capacitor input type of power supply is estimated as 800 Ω. The output resistance of the regulated supply is, from Fig. 8.25,

$$R_{out} = \frac{R_{in} + r_a}{1 + \mu Ak}.$$

For an anode working voltage of approximately 125 V, an A2293 has $r_a = 700\,\Omega$ and $\mu \doteqdot 4$. Also, $k \doteqdot V_{REF}/V_O \doteqdot 0{\cdot}5$ if an 85 V reference source is used.

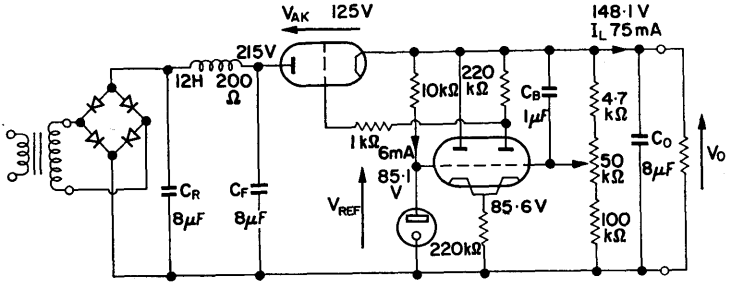



FIG. 8.26. Circuit arrangement of Design Example 8.5.

Thus,

$$R_{out} = \frac{800 + 700}{1 + 4 \times A \times 0{\cdot}5}.$$

From this, since $R_{out}$ is required to be 20 Ω, $A = 1500/40$; let it be made a minimum of 40.

The gain for a cathode coupled amplifier of the type shown in Fig. 8.26 is given by

$$A = \frac{\mu R_L}{2r_a + R_L} \quad \text{(see 6.4).} \tag{8.17}$$

To achieve a gain of 40 a large value of $R_L$ is required and the valve will necessarily be operated at a low current level. A valve which is suitable for operation under such conditions is the ECC83 high $\mu$ triode. If $A$ is assumed to be a signless quantity, then, from eqn. (8.17),

$$R_L = \frac{2r_a A}{\mu - A}.$$

Estimated values for $r_a$ and $\mu$, over the working range, are 100 kΩ and 80 respectively.

Thus,

$$R_L = \frac{2 \times 100\ \text{k}\Omega \times 40}{80 - 40} = 200\ \text{k}\Omega.$$

Let $R_L$ be the preferred value of 220 kΩ.

*Cathode resistor.* A value of 220 kΩ provides a low common mode gain while allowing a reasonable cathode current of 0·36 mA.

*Reference supply.* The 85A2 reference tube requires an operating current of 6 mA for optimum performance. This can be provided from the 150 V supply through a 10 kΩ resistor.

*Ripple voltage.* The 100 c/s ripple voltage has an estimated value of 1 V peak-to-peak at the output of the *L–C* filter. This

is reduced by the factor $1/\mu Ak$ to 12·5 mV by the action of the regulator. At the ripple frequency, $k$ can be made equal to unity by using a capacitor $C_B$ to bypass the voltage dividing chain. The magnitude of the ripple voltage is thus of the order of 6 mV at full load.

In Fig. 8.27 the output voltage of the regulator is plotted against load current. The broken line indicates the series valve grid–cathode voltage required to maintain the load current.

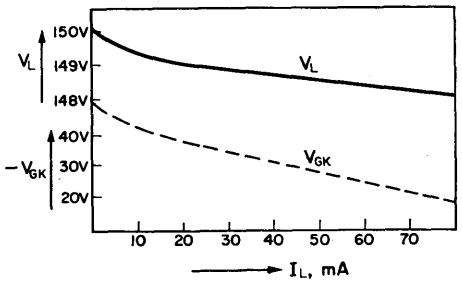



FIG. 8.27. Performance of Design Example 8.5. Output voltage is plotted against load current. The broken line indicates the series valve grid–cathode voltage $V_{GK}$ required to maintain the load current.

## 8.12. TRANSISTOR SERIES REGULATOR

It is a frequent requirement, particularly with transistor systems, to derive several low impedance voltage sources from the main supply rail.

### DESIGN EXAMPLE 8.6

Required, a transistor series regulator to provide 60 mA at $-5$ V from a $-15$ V stabilized supply. The nominal output impedance should be 0·1 Ω.

The excess voltage is developed across a compound emitter follower. Referring to Figs. 8.21 and 8.22, it is seen that the main change in output voltage from such a circuit, as the load current is varied, is due to the change in $V_{BE}$ required to maintain

the load current. In the circuit of Fig. 8.28 the output voltage is compared with a reference voltage, using a longtail pair. The difference voltage is amplified and applied to the series element so as to offset changes in $V_{BE}$.

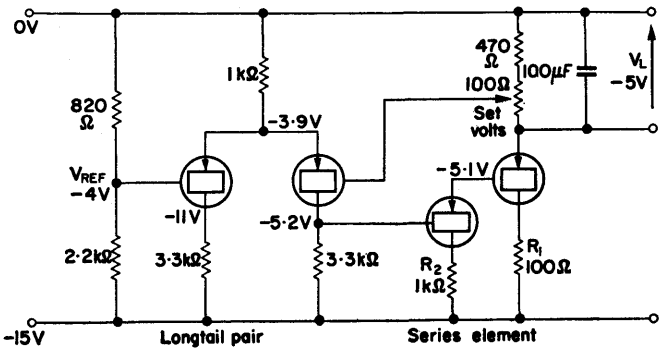



FIG. 8.28. Circuit diagram of Design Example 8.6.

*Series element.* The output transistor must be capable of dissipating 10 V × 60 mA = 600 mW. The maximum collector dissipation of an OC84 transistor with a cooling clip, and at 35 °C, is 350 mW. A series resistor in the collector will reduce the collector dissipation and also limit the current under short circuit conditions. A suitable value is 100 Ω which will drop 6 V of the 10 V excess voltage when the load current is 60 mA. This reduces the collector dissipation to 240 mW at full load.

If an OC44 is used to drive the output transistor, the overall current gain of the pair is 5000. As the input base current required for full load current is then only 12 μA, loading on the difference amplifier will be small. The output resistance $R_s$ of the series element is approximately 5 Ω, due to the change in $V_{BE}$ with load current.

*Difference amplifier.* The output resistance of the closed loop system is

$$R_{\text{out}} = \frac{R_s}{1 + A_v k},$$

where $R_s$ is the output resistance of the series element alone, and $k$ is the fraction of the output voltage fed back.

A suitable value for $k$ is 0·8, making $V_R = 0{\cdot}8\,V_0 = 4$ V. For $R_s = 5\,\Omega$, the voltage gain required to make $R_{out} = 0{\cdot}1\,\Omega$ is

$$A_v \doteqdot R_s/R_{out}\,k \doteqdot 63.$$

For a long tail pair,

$$A_v = \frac{g_m R_L}{2} \text{ [from eqn. (6.23)]},$$

or,

$$R_L = 2A_v/g_m = 3{\cdot}1\ \text{k}\Omega \quad (\text{for } g_m = 40\ \text{mA/V}).$$

Collector resistors of 3·3 kΩ ensure that the necessary gain is attained.

*Emitter resistor.* As the reference voltage is −4 V the emitter voltage will be slightly less negative at −3·9 V. A 1 kΩ emitter resistor fixes the total collector current at 4 mA. Transistor $T_2$

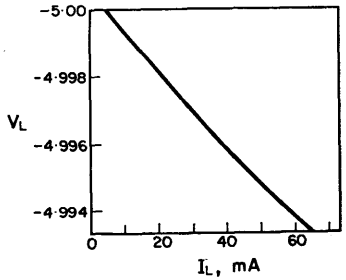



FIG. 8.29. Closed loop series stabilizer output voltage plotted against load current.

passes 3 mA to give a collector voltage of approximately −5 V required for the input of the compound emitter follower stage. The 1 mA in the other collector resistor produces a voltage of −11 V at the collector of $T_1$. Thus, both transistors are operating in the linear range.

In Fig. 8.29 output voltage is plotted against load current for the closed loop series stabilizer. It indicates a nominal output resistance of 0·09 Ω at the full load current of 60 mA.

## 8.13. Output Transistor Protection

If the output of a series stabilizer is short circuited, unless the current is limited, the output transistor can be destroyed by excessive dissipation. In the previous example, the collector

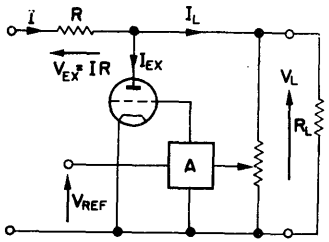



Fig. 8.30. Shunt stabilizing circuit. The output voltage controls the excess current drawn through the shunt element, such that under all load conditions $I$ is constant.

resistors protect the compound emitter follower stage, under overload conditions, by dropping the collector voltage and bottoming the transistors.

Another form of protection, commonly in use, employs a network that is switched by excessive current and reduces the input voltage of the series element to zero. The output transistor is reverse biased eliminating possibility of damage.

### *Shunt Stabilizers*

This family of regulators maintains the output voltage constant, by drawing a constant current from the supply. Referring to Fig. 8.30 the excess current, $I_{EX} = I - I_L$, is taken from the shunt element in a manner similar to a discharge tube supply.

The shunt element can be either a valve or a transistor. The excess voltage is dropped across $R$ which may be a separate resistor or the inherent resistance of the unregulated supply.

## 8.14. Constant Current Supplies

Just as a constant voltage supply can be obtained from an amplifier with voltage (shunt) feedback, a constant current supply can be obtained from an amplifier with current (series) operated feedback. This is discussed in Chapter 7. The constant current devices of Chapter 5 are elementary forms of such supplies.

CHAPTER 9

# Oscillators

## Introduction

An electronic oscillator may be described as a device which, whilst obtaining its power from a d.c. source, provides an alternating output without changing its circuit configuration by means of mechanical switching. Such a definition thus excludes rotating machinery and vibrators, etc.

Oscillators fall into two classes; firstly, those which provide a sinusoidal output, and secondly, "relaxation" types whose outputs have a large harmonic content. This latter class is dealt with in Chapter 10 on waveform generators.

## 9.1. Sinusoidal Oscillators—Basic Considerations

Figure 9.1 represents a current source having resistance $R_S$, feeding a parallel circuit of $R_L$, $C$ and $L$. The current $i(s)$ need not be a specific input but could be noise signals due to thermal agitation or switching transients, etc.

$$v(s) = Z \,.\, i(s) \tag{9.1}$$

$$= \frac{i(s)}{G_S + G_L + sC + (1/sL)}. \tag{9.2}$$

Multiplying through by $s/C$,

$$v(s) = \frac{i(s)\,(s/C)}{s^2 + [s(G_S + G_L)/C] + (1/LC)}. \tag{9.3}$$

The denominator of eqn. (9.3) is the characteristic equation of the circuit, and the performance of the circuit is principally determined by its roots. Thus, let

$$s^2 + \frac{s(G_S + G_L)}{C} + \frac{1}{LC} = 0. \tag{9.4}$$

Solving this equation,

$$s = -\left(\frac{G_S + G_L}{2C}\right) \pm j\sqrt{\left[\frac{1}{LC} - \left(\frac{G_S + G_L}{2C}\right)^2\right]}. \tag{9.5}$$

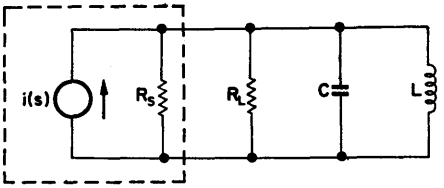



FIG. 9.1. A current source of resistance $R_s$, feeding a parallel circuit of $R_L$, $C$ and $L$.

There are therefore two roots of the form

$$s_1 = -\alpha + j\omega \quad \text{and} \quad s_2 = -\alpha - j\omega, \tag{9.6}$$

and the solution is

$$v(t) = A \exp(-\alpha + j\omega)\, t + B \exp(-\alpha - j\omega)\, t. \tag{9.7}$$

The nature of $s_1$ and $s_2$ is largely determined by the term $(G_S + G_L)$. Thus, if $(G_S + G_L) = 0$, $s = j\sqrt{(1/LC)}$ and denoting $1/LC$ by $\omega_0^2$,

$$s_1 = +j\omega_0 \quad \text{and} \quad s_2 = -j\omega_0.$$

Hence, for $G_S = G_L$,

$$v(t) = A \exp(j\omega_0 t) + B \exp(-j\omega_0 t), \tag{9.8}$$

and the solution represents an oscillation of $\omega_0$ radians per second, of constant amplitude.

More generally, where $(G_S + G_L)$ does not equal 0, given a disturbing signal, oscillations will commence if the roots $s_1$ and $s_2$ have imaginary parts, i.e. if in eqn. (9.5), $1/LC$ is greater than $[(G_S + G_L)/2C]^2$. Furthermore, the amplitude of oscillation will increase with time if $(G_S + G_L)$ is less than 0, which implies that $G_L$ is negative. The concept of a negative value of $G_L$ means that energy is supplied to overcome the loss resistance that is always associated with a tuned circuit.

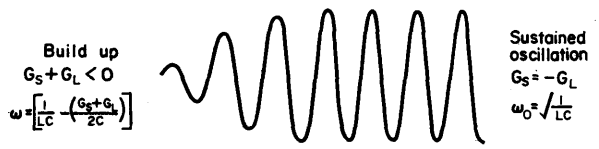



FIG. 9.2. Build-up of an oscillation. The condition for commencement of oscillation is that $G_s + G_L$ is negative, and the amplitude stabilizes when $G_s = -G_L$.

From these considerations, the requirements for a build-up of oscillation, as shown in Fig. 9.2, are as follows:

(a) A negative resistance component to compensate for tuned circuit losses and provide a divergent oscillation.
(b) A variable resistance component which reduces the real part of the roots to zero when the required amplitude is reached.
(c) A frequency determining element.
(d) An initiating signal.

## 9.2. NEGATIVE RESISTANCE

Defining a negative resistance as an element through which current decreases as the voltage across it increases, it may be represented on a current–voltage characteristic. Thus, in Fig. 9.3, the part of the curve lying between $A$ and $B$ is a negative resistance region having a slope of $-G$.

Any device whose current–voltage characteristics include such a region, possesses one of the requirements for oscillation, and by suitable circuit arrangement may be used as an oscillator.

As examples of such devices there are:

(a) Dynatron Oscillator using the tetrode negative resistance characteristic.
(b) The Transitron Oscillator using a pentode with screen and suppressor grids connected.
(c) Solid state devices such as point-contact transistors, thermistors and tunnel diodes.

The Dynatron and Transitron oscillators are now mostly of historical interest, but the tunnel diode is becoming widely used for high frequency oscillators in the range 100 Mc/s to 10 kMc/s.

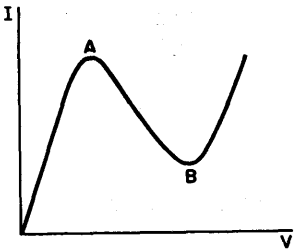



FIG. 9.3. Current–voltage curve showing a negative resistance region $AB$, where, as the voltage increases the current decreases.

Alternatively, a negative resistance can be obtained by feedback connection of an amplifier. From eqn. (7.6), the output impedance of an amplifier with feedback is written as:

$$Z_{\text{out}} = \frac{Z_{OA}}{1 - A\beta}, \tag{9.9}$$

which is negative for a loop gain $A\beta$ greater than unity. It is this method of obtaining negative resistance which is now most commonly used in the design of oscillators.

Sinusoidal oscillators of the feedback type fall into two classes, inductance–capacitance types, and resistance–capacitance (phase-shift) types. These are considered in detail later in this chapter.

## 9.3. Amplitude Stabilization

It was shown in § 9.1 that for oscillations to build up it is necessary that $G_L$ should be negative and greater than $G_S$. In other words, the damping term of eqn. (9.4) should be negative. In addition the value of $G_L$ must decrease with increasing amplitude of oscillation until, at the required amplitude, $G_S = -G_L$, making the damping term zero.

Alternatively, referring to eqn. (9.9) for feedback amplifiers, for the build-up condition the loop gain $A\beta$ should be greater than unity, and decrease until it reaches unity when the correct amplitude of oscillation is reached. Given a constant feedback factor $\beta$, this implies that the amplifier gain must decrease as the signal amplitude increases, and to achieve this some non-linear element is necessary.

### *Grid Leak Stabilization*

In tuned $L$–$C$ oscillators, a common method of varying gain with signal amplitude, and thus providing oscillator limitation, is by the use of a grid leak. The required non-linearity is provided

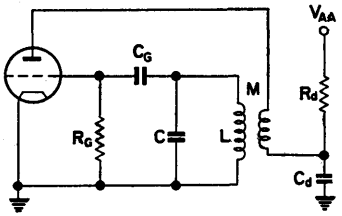



FIG. 9.4. Circuit diagram of a tuned grid oscillator employing grid leak amplitude stabilization. $R_D$ and $C_D$ are decoupling elements.

by the bottom bend of the valve $I_A/V_G$ characteristic. In Fig. 9.4 which represents a tuned grid oscillator, $C_G$ and $R_G$ form the grid leak combination, the time constant of which is chosen to be much greater than the period of oscillation $1/f$. It should not, however, be so great that changes in operating conditions cannot

be accepted without affecting circuit performance. In this example, which is typical of a local oscillator for a superheterodyne receiver at medium frequency, say 1 Mc/s, suitable values would be $R_G = 1\ \text{M}\Omega$, and $C_G = 100\ \text{pF}$, with a time constant of $10^{-4}$ sec. This is sufficiently long compared with the oscillatory period of $0{\cdot}68 \times 10^{-6}$ sec for a local frequency of 1·45 Mc/s.

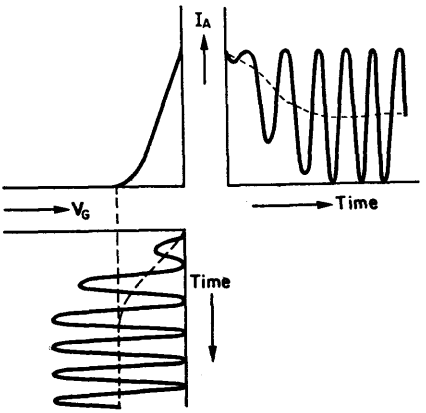



FIG. 9.5. Build up of oscillation with grid leak amplitude stabilization, after the oscillator is switched on at time $t = 0$.

The amplitude stabilizing effect of the grid leak may best be explained with reference to Fig. 9.5 showing a typical build up of oscillation. The effective $g_m$ is given by the slope of the $I_A/V_G$ curve, which is high at $V_G = 0$ and becomes progressively lower as the grid bias is carried more negative. The grid bias is determined by the charge on $C_G$. Grid current flows on positive peaks of grid signal voltage and charges the capacitor. Due to the $CR$ time constant the charge is additive, and the bias is carried negative thus reducing the gain of the amplifier. The process continues until the $g_m$ is just sufficient to maintain oscillation when the amplitude stabilizes. Should now the gain become reduced, instantaneously the positive signal peaks would cease to carry the grid positive with respect to the cathode, and no

grid current would flow. Some part of the charge on $C_G$ would then leak away, and the effective grid bias would be reduced until the positive peaks again caused grid current to flow. Operation would then stabilize at a smaller amplitude of oscillation.

This form of operation is under class C conditions with the operating grid bias beyond cut-off. It causes a discontinuous anode current to flow, but a tuned circuit having a reasonably high $Q$ ensures that the anode voltage is sinusoidal, by providing a low impedance path for harmonic frequencies.

*Squegging*

At the point of amplitude-stable-oscillation, the time constant is such that, the amount of charge leaking away from the capacitor between positive signal peaks is just equal to the amount that is restored when grid current flows. If the time constant is too great, and signal amplitude is excessive, more charge is supplied by grid current than is allowed to leak away between peaks, and the valve is quickly biased to a negative voltage much greater than the cut-off point. Anode current then ceases and oscillations cannot be maintained. The capacitor gradually discharges through the grid leak resistor, until the bias is low enough to allow anode current to flow and oscillations to recommence. The cycle repeats itself and results in intermittent bursts of oscillations known as *squegging*. This condition can normally be prevented by careful choice of grid leak values. When the oscillator is used in a radio receiver, a large h.t. decoupling resistor also helps to prevent it. Such a resistor causes the oscillator anode voltage to rise with a decrease in anode current, thus moving the cut-off voltage to a higher negative value.

## 9.4. Survey of Feedback *L–C* Oscillators

The most general type of oscillator is the tuned anode–tuned grid arrangement shown in Fig. 9.6. Only the signal paths are drawn, and feedback is seen to be via the anode to grid capacitance. Figure 9.7 similarly represents four commonly encoun-

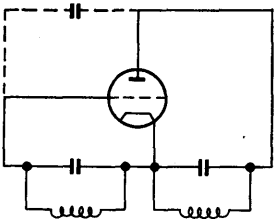
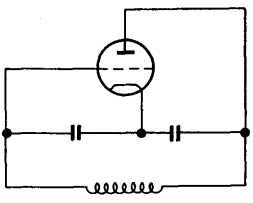


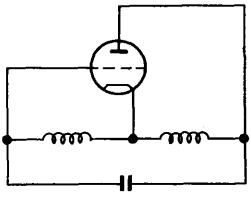
FIG. 9.6. Tuned anode–tuned grid oscillator. Feedback is present through $C_{ag}$ the anode to grid capacitance.



$\omega^2 = 1/L\,\frac{C_1 C_2}{C_1+C_2}$

$g_m = g_a C_2/C_1$

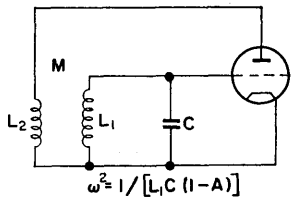
(a) Colpitts



$\omega^2 = \frac{1}{(L_1-L_2-2M)C}$

$\mu = (L_1+M)/(L_2+M)$

(b) Hartley

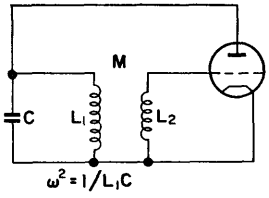



$\omega^2 = 1/[L_1C\,(1-A)]$

$M = -\left[\frac{L_2 A}{\mu(1-A)} + \frac{CR}{g_m}\right]$

Where R is the effective series primary resistance, and $A = L_2R/L_1r_a$

(c) Tuned grid




$\omega^2 = 1/L_1C$

$g_m = \frac{L}{M}(g_a - G)$

Where G is the shunt conductance across the tuned circuit

(d) Tuned anode

FIG. 9.7. Four commonly encountered oscillator types.

tered oscillators which are variations on this basic circuit arrangement.

Associated with each circuit are the relevant equations defining the frequency and the conditions for maintenance of oscillation.

The tuned transformer types of oscillator are extensively used as local oscillators in radio receivers. The tuned anode is more stable to h.t. fluctuations than is the tuned grid and in addition has less harmonic content and provides a greater amplitude output. The tuned grid, however, has a more constant amplitude when the oscillator frequency is varied over its tuning range. For use at v.h.f. the Colpitts type is usually preferred, although the Hartley oscillator may also be used at frequencies in excess of 40 Mc/s. Two common ways of obtaining the operating conditions for these circuits are:

(a) to find the condition under which the loop gain is unity,
(b) to determine the nodal or circuital equations and equate the determinant to zero. (A brief introduction to determinants is given in Appendix A.)

Both methods are demonstrated in the two design examples which follow.

## 9.5. The Tuned Anode Oscillator

Two circuit arrangements of the tuned anode oscillator are given in Fig. 9.8. They differ in the manner in which h.t. is fed to the anode. In the parallel feed case the effect of $R$ is to reduce

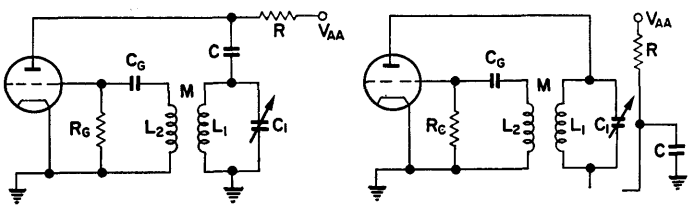



FIG. 9.8. Shunt and series fed tuned anode oscillators.

amplitude variation, as the frequency is changed, but has the disadvantage that it damps the tuned circuit.

*Design Considerations*

To determine the operating conditions the circuit of Fig. 9.7d is redrawn as the small signal equivalent network of Fig. 9.9, in

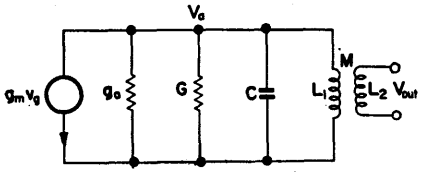



FIG. 9.9. Small signal equivalent network of Fig. 9.7d.

which $G$ represents the effective shunt conductance across the tuned circuit. The equations of this network are written as:

$$-g_m v_g = v_a\left(g_a + sC + G + \frac{1}{sL}\right),$$

$$v_{out} = -\frac{sM}{sL_1}v_a = -\frac{M}{L_1}v_a.$$

For unity loop gain, $v_0 = v_g$ and

$$\frac{M}{L_1}g_m + g_a + sC + G + \frac{1}{sL_1} = 0.$$

Multiplying through by $sL_1$,

$$sMg_m + sL_1g_a + s^2L_1C + sL_1G + 1 = 0,$$

and in terms of real frequency,

$$-\omega^2L_1C + 1 + j\omega(L_1g_a + L_1G + Mg_m) = 0.$$

Equating real components,

$$\omega^2 = 1/L_1C. \tag{9.10}$$

Equating imaginary components,

$$g_m = -\frac{L_1}{M}(g_a + G). \tag{9.11}$$

Thus, the circuit will oscillate at a frequency $f = 1/[2\pi\sqrt{(LC)}]$ if the effective $g_m$ of the valve is $-(L_1/M)(g_a + G)$. In this latter expression, the negative sign is associated with the mutual inductance and indicates that oscillation will only occur for one connection of the feedback winding.

Tight coupling and low values of $M$ are helpful in maintaining frequency stability. However, the tuned circuit should have a high $Q$ to reduce the harmonic content of the oscillation and accordingly $L_1$ (in Fig. 9.9) is made large. Since $M = k\sqrt{(L_1L_2)}$, this implies a low value of $L_2$. Another consideration which requires that the grid inductance should be small is that, with the stray capacitances associated with it, its resonant frequency should be much greater than the highest frequency at which the circuit is to oscillate. Methods have been suggested[30] for calculating the inductance of the feedback winding but these in general yield values somewhat smaller than required. In practice, the number of turns of the feedback winding is initially made one-third to one-half of the number of turns of the main winding. This usually gives an inductance greater than that actually required and the final adjustments are made experimentally.

*Choice of a Valve*

The choice of a valve for use as a local oscillator in a radio receiver is somewhat limited because composite valves are commonly employed. As an example the ECH81 triode-heptode has a triode section specifically designed to have the correct characteristics for use as an oscillator, while the heptode section is used for frequency changing purposes. The valve manufacturer's data sheets usually indicate the correct electrode voltages, leak resistance and grid current required when such a valve is to be used as an oscillator. Where a separate valve is to be used, one should be chosen having a high value of $g_m$ and $r_a$. A high $r_a$

tends to make the frequency of oscillation more independent of valve parameters, and hence more stable, while a high value of $g_m$ provides greater ease of oscillation.

*Design Steps*

1. Calculate the inductance which, with the selected variable capacitor, will resonate over the required frequency range.
2. Make the grid winding have one-half the turns of the primary winding. Since inductance is proportional to the square of the turns, $L_2$ is thus $L_1/4$.
3. Determine the value of $G$, the effective shunt conductance across the tuned circuit, and with a knowledge of the effective $g_m$ and $r_a$ of the valve, from eqn. (9.11) evaluate $M$.
4. Knowing $M, L_1$ and $L_2$, calculate the coupling coefficient $k$.
5. Choose $C_G$ which with the recommended grid leak resistor will have a time constant 4 or 5 times $1/f_{\text{min}}$.
6. Select an anode resistor to give the correct operating anode voltage and decouple it.

DESIGN EXAMPLE 9.1

Required, a series fed, tuned anode oscillator using the triode section of an ECH81, covering the frequency range 1–2 Mc/s. The supply voltage is 250 V.

From the valve data sheets, with $V_A = 100$ V, recommended operating conditions are obtained with $I_G = 200\ \mu$A and $R_G = 47$ kΩ. The effective $g_m$ is given as 650 μA/V, $r_a = 6$ kΩ, and the mean anode current $I_A = 4{\cdot}5$ mA.

Let the selected variable capacitor, with strays, tune over the range 50–450 pF. With an inductance of 100 μH, a frequency range of approximately 760 kc/s to 2·2 Mc/s is obtainable, which meets the specification. Thus, $L_1 = 100\ \mu$H and initially make $L_2 = L_1/4 = 25\ \mu$H.

For a $Q$ of 100 at the top frequency of 2 Mc/s, the resistance of $L_1$ is $r = \omega L/Q \doteqdot 12{\cdot}5\ \Omega$. The effective shunt conductance across the tuned circuit is $Cr/L$, which is 6·25 μmhos at $C = 50$ pF and 56·25 μmhos at $C = 450$ pF.

From eqn. (9.11) for maintenance of oscillation, $M$ should equal or be greater than $(g_a + G)L/g_m$. If the condition is satisfied for the larger value of $G$ it will be satisfied over the whole tuning range. Thus, since $r_a = 6\ \text{k}\Omega$, $g_a = 166\ \mu\text{mhos}$,

$$M = \frac{(166 + 56) \times 10^{-6} \times 100 \times 10^{-6}}{650 \times 10^{-6}} = 34\ \mu\text{H}.$$

The coefficient of coupling

$$k = \frac{M}{\sqrt{(L_1 L_2)}} = \frac{34 \times 10^{-6}}{\sqrt{100 \times 25 \times 10^{-12}}} = 0{\cdot}68.$$

*Grid leak.* At the lowest frequency of 1 Mc/s, $1/f = 1\ \mu\text{sec}$. From the data sheet, the recommended value for $R_G$ is 47 kΩ.

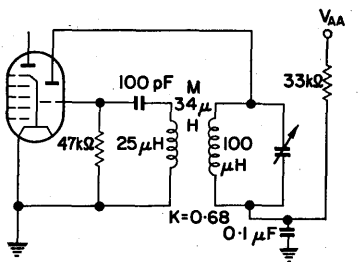



FIG. 9.10. Completed circuit diagram of Design Example 9.1.

If this is used with a capacitor of 100 pF a time constant of 4·7 μsec is obtained which is sufficiently long.

*Anode decoupling.* For a $V_A$ of 100 V from an h.t. of 250 V the anode resistor must drop 150 V at the mean anode current of 4·5 mA.

Thus,

$$R = 150/4{\cdot}5 = 33\ \text{k}\Omega.$$

A 0·1 μF capacitor is suitable for decoupling and the completed circuit is given in Fig. 9.10.

This treatment has been simplified in order to show the basic approach to oscillator design. No attempt has been made to obtain constant amplitude over the tuning range, nor has provision been made for the "tracking" which would be necessary in a radio receiver local oscillator. An excellent treatment leading to the design of the more sophisticated circuit to meet these requirements is given by Sturley.[16]

## 9.6. Colpitts Oscillator (Transistor)

In the case of the valve oscillator it was shown that some non-linearity was required to limit the amplitude of oscillation after the build-up period, and the bottom bend of the $I_A/V_G$ characteristic served this purpose. In a similar manner, when using a transistor, a non-linearity is introduced by allowing the transistor to bottom.

The basic circuit arrangement is given in Fig. 9.11, and the frequency of oscillation is determined by the combination of $L$,

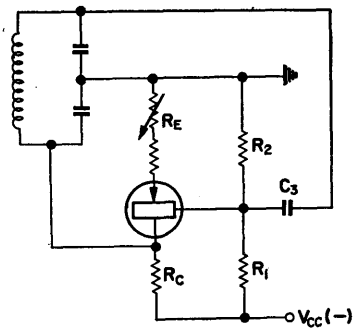



Fig. 9.11. Colpitts transistor oscillator.

$C_1$ and $C_2$. $L$ is provided with an iron dust core to permit accurate frequency adjustment. $R_1$, $R_2$ and $R_E$ give the correct bias conditions, and the variable part of $R_E$ is adjusted to obtain an acceptable waveform.

*Design Considerations*

In this example the conditions for oscillation are determined using method (b) of § 9.4. An approximate equivalent network is drawn in Fig. 9.12 in which $G_1$ is the conductance of the collector resistor and $R_B$ represents the effective parallel combination of $R_1$ and $R_2$.

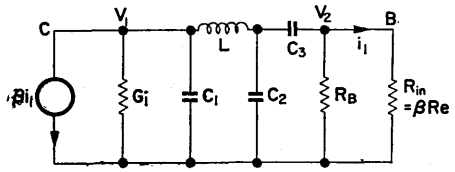



FIG. 9.12. Approximate equivalent network of the Colpitts transistor oscillator. The coupling capacitor $C_3$ isolates the collector d.c. voltage from the base and is ignored in analysis.

To a first approximation $r_{in}$ may be considered as being supplied from a constant voltage source $V_2$. The effective $g_m$ of the transistor is then

$$g'_m = \beta/r_{in} \doteqdot \beta/\beta R_E \doteqdot 1/R_E \quad \text{[from eqn. (2.35)]}. \qquad (9.12)$$

If $C_3$ is very large it may be neglected and, writing $G_2$ for the conductance of the parallel combination of $R_B$ and $r_{in}$, the equations of the network are:

$$\left(G_1 + sC_1 + \frac{1}{sL}\right) v_1 - \frac{1}{sL} v_2 = -g_m v_2,$$

$$-\frac{1}{sL} v_1 + \left(\frac{1}{sL} + sC_2 + G_2\right) v_2 = 0.$$

The determinant is:

$$s^3 LC_1C_2 + s^2(LC_1G_2 + LC_2G_1) + s(LG_1G_2 + C_1 + C_2) + G_1 G_2 + g_m = 0.$$

Writing this expression in terms of real frequency and equating imaginary terms to zero,

$$\omega^2 = \frac{[LG_1G_2/(C_1 + C_2)] + 1}{LC_1C_2/(C_1 + C_2)} \doteqdot \frac{1}{LC_1C_2/(C_1 + C_2)}$$

$$\left(= \frac{1}{\frac{1}{2}LC} \quad \text{if} \quad C_1 = C_2\right). \tag{9.13}$$

Equating real terms to zero and substituting for $\omega$,

$$g_m = \frac{G_1C_2^2 + G_2C_1^2}{C_1C_2} \; (= G_1 + G_2 \quad \text{if} \quad C_1 = C_2). \tag{9.14}$$

As $r_{in}$ is much greater than $R_B$, $G_2 \doteqdot 1/R_B$.

Hence for the case where $C_1 = C_2$,

$$g'_m = 1/R_B + 1/R_C.$$

But, from eqn. (9.12),

$$g'_m = 1/R_E,$$

Therefore

$$1/R_E = 1/R_B + 1/R_C. \tag{9.15}$$

*Choice of Transistor*

The main consideration is that of the cut-off frequency of the transistor. Commonly, r.f. transistors are used in fixed frequency oscillator circuits up to 1·25 times the cut-off frequency, while in variable frequency oscillators the limit is usually about 0·8 times $f_\alpha$.

*Design Steps*

1. Using expression (9.13), select values for $L$, $C_1$ and $C_2$ to obtain the desired frequency of oscillation.
2. Set up the correct bias conditions by suitable choice of $R_1$

and $R_2$ which, with $R_E$, will determine the mean collector current.

3. Select the value of $R_C$ and using eqn. (9.15) calculate $R_E$.

DESIGN EXAMPLE 9.2

Required, a Colpitts oscillator operating at 500 kc/s, and using an OC44 transistor. A supply voltage of $-9$ V is available.

*The tuned circuit.* The collector capacitance is effectively across the tuned circuit and is a function of collector voltage. To obtain frequency stability independent of the collector capacitance the tuned circuit capacitors should be relatively large. Let $C_1 = C_2 = 1000$ pF.

From eqn. (9.13),

$$L = 2/\omega^2 C = 200\ \mu\text{H}.$$

*D.C. biasing.* This may be done using emitter resistor stabilization as described in § 2.11. A voltage divider of $R_1 = 10$ kΩ and $R_2 = 2{\cdot}2$ kΩ will provide a base voltage of $-1{\cdot}5$ V and ensures a low d.c. resistance for the base supply. The collector current is then a function of the emitter resistor, and the emitter voltage is also about $-1{\cdot}5$ V. Let the mean collector current be initially chosen as 2 mA. With a collector resistor of 2·7 kΩ, the mean collector voltage will be $-4{\cdot}6$ V and will thus be able to swing between $-1{\cdot}5$ and $-7{\cdot}7$ V without distortion.

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{22 \times 10^3}{12{\cdot}2} = 1{\cdot}8\ \text{k}\Omega.$$

From eqn. (9.15),

$$R_E = \frac{R_B R_C}{R_B + R_C} = \frac{1{\cdot}8 \times 2{\cdot}7 \times 10^3}{4{\cdot}5} = 1{\cdot}08\ \text{k}\Omega.$$

Let $R_E$ be made up of a 330 Ω fixed resistor and a 1 kΩ variable resistor. Final adjustment of the circuit is made by varying this resistor until oscillation is just taking place. This avoids the distortion of the waveform which would otherwise occur if the transistor was overdriven.

## 9.7. Resistance–Capacitance Oscillators

Due to the size of high value inductances, *R–C* oscillators have, in the past, been preferred to *L–C* types for operation at low frequencies. In fact, the use of modern ferrite materials now enables such inductances to be made physically small, so this consideration is no longer of such importance.

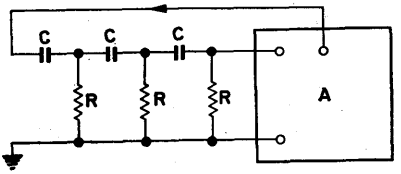



FIG. 9.13. The arrangement of a phase shift oscillator. The *C–R* network provides a phase shift of 180° and the required amplifier gain is −29.

The two most common types of *R–C* oscillators are:

(a) *Phase shift.* This type of oscillator is illustrated in Fig. 9.13. The feedback network provides a phase shift of 180° at the frequency of oscillation. It can be shown that in this circuit, for equal capacitors and resistors, infinite input impedance and zero output impedance of the amplifier, the condition for maintenance of oscillation is that the gain should be −29. This is the gain required to compensate for the attenuation of the phase shifting network. The frequency of oscillation of the phase-shift oscillator set up in this manner is $f = 1/(2\pi RC\sqrt{6})$. Tapered networks using different values of $C$ and $R$ and the addition of an extra phase-shifting stage can reduce the attenuation of the feedback path.

(b) *Bridge type.* The feedback network of the bridge type oscillator provides zero phase shift at the frequency of oscillation. A typical circuit is that of the Modified Wien Bridge which is treated in detail in the next section.

## 9.8. Modified Wien Bridge Oscillator

For wide range tuneable oscillators the Wien Bridge (or one of its modifications) is frequently used for operation from 1 to $10^7$ c/s. This type of oscillator provides a range of frequency

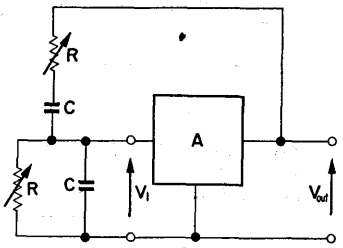



FIG. 9.14. Arrangement of a Wien bridge oscillator. The *R–C* network provides zero phase shift at the frequency of operation and the required amplifier gain is 3.

variation which is much greater than can be obtained from *L–C* type oscillators.

### *Design Considerations*

Figure 9.14 illustrates the basic circuit arrangement. Writing $T = CR$, the forward voltage transfer function for the feedback network is:

$$\frac{v_{in}}{v_{out}} = \frac{sT}{(sT)^2 + 3sT + 1},$$

which is the feedback factor $\beta$.

The condition for maintenance of oscillation is that the loop gain, $A\beta$ should be unity. That is,

$$\frac{j\omega TA}{(j\omega T)^2 + 3j\omega T + 1} = 1$$

or

$$\omega^2 T^2 + (A - 3) j\omega T - 1 = 0.$$

Equating imaginary terms to zero,

$$A = 3. \tag{9.16}$$

Equating real terms to zero,

$$\omega = 1/CR. \tag{9.17}$$

Thus if the amplifier has zero phase shift, infinite input resistance and zero output resistance, it is required to have a gain of 3 and the frequency of oscillation is given by $\omega = 1/CR$. Since $L$–$C$ oscillators have their frequency inversely proportional to the square root of $LC$ the Wien Bridge circuit can obviously provide a wider frequency range, and it is for this reason that it is generally preferred for use in laboratory type instruments. By using a ganged variable resistor, a 10 to 1 variation in frequency is readily obtained. In practice it is difficult to obtain perfect matching of the resistors over the complete range, and the amplifier will certainly have a finite output impedance. In addition the gain of the amplifier is likely to vary with frequency, so that it is probable that at some point in the tuning range the conditions for maintenance of oscillation will not be met. To ensure that this does not happen, thus causing oscillations to cease, a non-linear element is usually included in the circuit, acting in such a manner that the gain of the amplifier is always maintained at a suitable level.

*Design Steps*

1. Design an amplifier having a gain of 3 and with nominally zero phase shift through it.
2. From eqn. (9.17) calculate values of $C$ and $R$ to obtain the correct frequency or range of frequencies.
3. Provide some non-linear element to stabilize the amplifier gain and thus to maintain the conditions required for oscillation.

DESIGN EXAMPLE 9.3

Required, a modified Wien bridge oscillator covering the frequency range 1 to 10 kc/s.

*The amplifier.* A suitable amplifier to provide a gain of 3 without signal inversion is the common-cathode type described in § 6.4, and illustrated in Fig. 9.15. The gain of such an amplifier is:

$$A = \frac{\mu R_L}{[r_a(r_a + R_L)/(\mu + 1)\,R_K] + 2r_a + R_L}$$

$$= \frac{\mu R_L}{2r_a + R_L} \quad \text{(for large } R_K\text{)} \tag{9.18}$$

$$= \frac{\mu(\mu + 1)\,R_K R_L}{r_a(r_a + R_L)} \quad \text{(for small } R_K\text{)}. \tag{9.19}$$

Let the valve chosen be a 12AT7 having $r_a = 10\,\text{k}\Omega$ and $\mu = 50$, and make $R_L = 20\,\text{k}\Omega$.

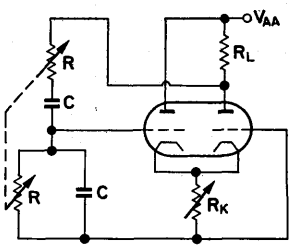



FIG. 9.15. The modified Wien bridge circuit of Design Example 9.3.

Substituting these values in eqn. (9.19) yields that $0{\cdot}12R_K = 3$. Thus, for initiation of oscillation, $R_K = 25\,\Omega$. An increase in this value initially causes the oscillator to be overdriven and a distorted waveform results.

However, a further increase in $R_K$ causes a reduction in gain due to the increase in cathode bias voltage, $V_K = I_K R_K$, and in

practice $R_K$ is increased from its minimum value until a satisfactory waveform is obtained.

*Frequency.* Let the selected ganged potentiometer have a maximum value of 50 kΩ. $R$ will be maximum at the lowest frequency, 1 kc/s. Thus, $C = 1/\omega R = 3184$ pF; make it 3300 pF.

*Gain stabilization.* In the completed circuit of Fig. 9.16 gain stabilization is achieved by applying negative feedback to the

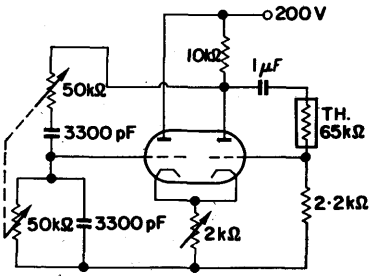



FIG. 9.16. Completed circuit of Design Example 9.3.

second half of the valve via a thermistor. $C_1$ serves as a blocking capacitor, keeping the anode voltage off the grid.

A thermistor is a non-linear device having a high negative temperature coefficient of resistance, and in this circuit its stabilizing action is as follows. An increase in amplifier gain causes the anode voltage to rise, leading to an increase in current through the thermistor. The resulting increase in temperature reduces the thermistor resistance, which increases negative feedback thus tending to restore the original gain.

## 9.9. MULTI-RANGE MODIFIED WIEN BRIDGE USING TRANSISTORS

*Design Considerations.*

As transistors are essentially current operated devices conditions for the maintenance of oscillation may most conveniently

be established by consideration of current flow, instead of voltage as was done in the previous example. Thus, drawing the feedback network as in Fig. 9.17, the current transfer function may be written as:

$$\frac{i_1}{i_2} = \frac{R/(1 + sCR)}{[R/(1 + sCR)] + [(1 + sCR)/sC]}.$$

Denoting $CR$ by $T$,

$$\frac{i_1}{i_2} = \frac{sT}{1 + 3sT + (sT)^2}.$$

This is of the same form as the basic equation developed for the valve circuit. If $i_1$ is the input current and $i_2$ is the output current of an amplifier of gain 3, the system will oscillate at a

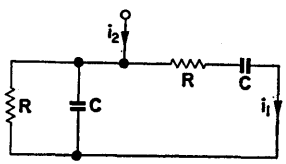



FIG. 9.17. Current, zero phase shift network. For $\omega = 1/CR$, $i_1$ and $i_2$ are in phase.

frequency of $\omega = 1/CR$ radians per second. The design steps for this circuit are thus the same as those of the previous example.

DESIGN EXAMPLE 9.4

Required, a modified Wien bridge transistor oscillator covering the frequency range 30 c/s to 30 kc/s.

*Current amplifier.* A suitable arrangement is a two-stage transistor amplifier with current feedback. This has the required properties of low input resistance and high output resistance, and is illustrated in Fig. 9.18. It is desirable that the input resistance should be much less than $R$ and the output resistance much greater than $R$. Under these conditions $i_2$ is assumed to be provided from a constant current source.

The gain of the amplifier with feedback is $A/(1 - A\beta)$, and if $A$ is sufficiently high this equals $1/\beta$. Thus, for maintenance of oscillation, $\beta = 1/3$. The feedback factor $\beta$, in this circuit is $R_2/(R_1 + R_2)$ so that $R_1$ must be made equal to twice $R_2$. For

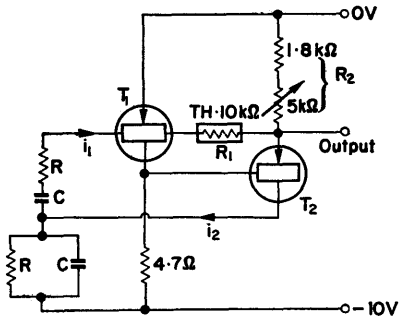



FIG. 9.18. Circuit diagram of Design Example 9.4.

this application 2 G 306 alloy type transistors are suitable and these can be directly coupled as shown. For a supply voltage of $-9$ V, a nominal current of 2 mA is reasonable for $T_1$. A larger current would require a lower value collector resistor, and this would cause an appreciable reduction in gain because of the high input resistance of $T_2$. In order to provide an output voltage of 1 V peak-to-peak, a relatively high value for $R_2$ is required.

*Frequency determining components.* Let the frequency requirement be provided by three ranges, 30–300 c/s, 300 c/s to 3 kc/s and 3–30 kc/s, and consider firstly the low frequency range. Make $C = 0{\cdot}5\ \mu$F, so that at 300 c/s, $R = 1/\omega C = 1{\cdot}06$ kΩ. Similarly, at 30 c/s, $R = 10{\cdot}6$ kΩ. The resistance component of the network may therefore be made up of a fixed resistor of 1 kΩ and a variable 10 kΩ resistor in series, as shown in Fig. 9.19. The two variable resistors are ganged, as are the two rotary switches which select the capacitors to be used. By making $C = 0{\cdot}05\ \mu$F

the oscillator will tune over the range 300 c/s to 3 kc/s, while for the range 3–30 kc/s a 0·005 μF is required.

*Gain stabilization.* Gain stabilization is achieved by the use of a non-linear feedback circuit as was done in Design Example 9.3. $R_1$ is a 10 kΩ thermistor and, being twice the nominal value

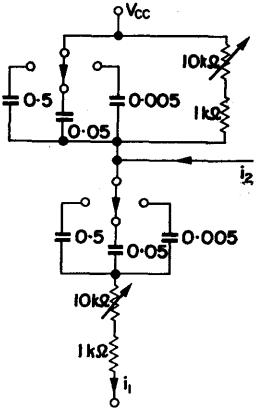



FIG. 9.19. Frequency determining network of Design Example 9.4.

of $R_2$, fulfils the condition for the maintenance of oscillation. The variable part of $R_2$ permits final circuit adjustments to be made.

## 9.10. FREQUENCY STABILITY

If the loop gain $A\beta$ of an oscillator is unity the circuit will oscillate, and the frequency of oscillation will be that at which the phase shift round the loop is zero. Should any change take place in the phase angle of $A\beta$ then the frequency of oscillation will automatically take up a new value at which the loop phase shift is again zero. Thus for good frequency stability a network should be used which, for a small change in frequency, provides a large change in phase angle. A resonant $L$–$C$ circuit has this

feature which improves as $Q$ is increased. Figure 9.20 represents the equivalent network of a quartz crystal, and such a device might typically have a $Q$ one thousand times as great as an $L$–$C$ tuned circuit operating under the same conditions. It is for this reason that quartz crystals are used where a fixed frequency is required with very good frequency stability.

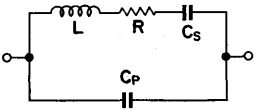



FIG. 9.20. Equivalent network of a quartz crystal.

*The Series Resonant Oscillator*

A crystal, as represented by Fig. 9.20, has two main resonant frequencies.

(a) Series resonance with $L$ and $C_s$.
(b) Parallel resonance with $L$ and $C_p$.

For maximum stability the series resonant condition is normally preferred for both crystal and $L$–$C$ circuits. This is because at series resonance the circuit has low impedance and is consequently less affected by external loading than is the high impedance parallel circuit. In the circuit of Fig. 9.21 representing

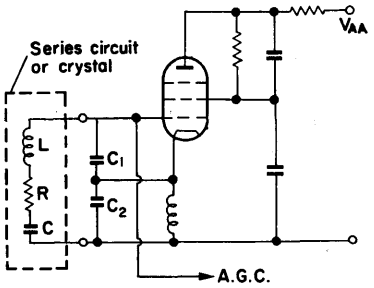



FIG. 9.21. Series resonant oscillator. The values of $C_1$ and $C_2$ are much greater than $C$.

a series resonant oscillator, the frequency determining elements may be either a series tuned circuit or a crystal. Other special steps, taken to improve frequency stability are

(a) the use of cathode feedback to eliminate Miller capacitance, and
(b) the use of low reactances across the valve input and output, to mask changes in valve capacitances.

Sandeman[31] has shown that the input impedance of the valve circuit, looking into the series combination of $C_1$ and $C_2$, is:

$$Z_{in} = -jX_1 - jX_2 - X_1X_2g_m,$$

the third term of which represents a negative resistance. Thus, as established in § 9.1, for oscillations to build up, this negative resistance should be greater than $R$, the resistance of the series tuned circuit (or crystal). The condition for maintenance of constant amplitude oscillation is that it should equal $R$, and the frequency of oscillation is given by:

$$f = \frac{1}{2\pi\sqrt{LC}}\sqrt{\left(1 + \frac{C}{C_1} + \frac{C}{C_2}\right)}. \qquad (9.20)$$

EXAMPLE. Let the series tuned circuit be made up of a capacitor $C = 250$ pF and an inductance $L = 100\ \mu$H having resistance $R = 5\,\Omega$. The resonant frequency of the circuit is thus 1 Mc/s. If $C_1 = 3000$ pF, and $C_2 = 10{,}000$ pF, then from eqn. (9.20),

$$f = 1 \text{ Mc/s} \times \sqrt{(1 + 0{\cdot}083 + 0{\cdot}025)} = 1{\cdot}053 \text{ Mc/s}.$$

At this frequency, $C_1$ has a reactance of approximately 50 Ω, and the reactance of $C_2$ is 15 Ω.

Equating the negative resistance to the resistance of the tuned circuit,

$$X_1X_2g_m = R; \quad 750\,g_m = 5 \quad \text{and} \quad g_m = 6{\cdot}6 \text{ mA/V}.$$

Thus a valve is required having an effective $g_m$ of 6·6 mA/V, and the frequency of oscillation is 1·053 Mc/s.

If a crystal is used instead of the series $L$–$C$ circuit, the value of $R$ might typically have a value of 100 Ω as compared to the 5 Ω of the inductance in this example. Different values of $C_1$ and $C_2$ are then required; these capacitors being given values as large as possible consistent with the conditions for maintenance of oscillation. The cathode inductance $L_2$ is chosen having a low d.c. resistance and a reactance high compared with the reactance of $C_2$.

*Automatic Gain Control*

As in previous examples it is necessary that the valve $g_m$ should be large enough to satisfy the condition for build-up of oscillation, falling to a lower value for constant-amplitude-operation. The use of automatic gain control with a variable-mu pentode meets this requirement, and enables the valve to be operated under Class A conditions. Automatic gain control is used in all cases where an extremely low harmonic content of the output waveform is required, another factor contributing to frequency stability. To provide the automatic gain control, the output signal is amplified and rectified, in some auxiliary circuit, and then fed back as a d.c. voltage which controls the bias, and hence the $g_m$ of the valve.

## 9.11. The Tunnel Diode Oscillator

Figure 9.22 represents the voltage–current characteristic of a typical tunnel diode, the region between $P$ and $V$ displaying the properties of negative resistance. Provided that the diode is operated in this region it may be used as the active element of an oscillator, and, due to its very low inherent capacitance, frequencies in the range 100 Mc/s to 10 kMc/s are possible. The small signal equivalent network of a tunnel diode, when suitably biased to operate in its negative resistance region, is given in Fig. 9.23. The effective negative resistance shunts the junction capacitance $c$, and this parallel combination is in series with $r_s$ the series resistance of the diode and $l_s$ the lead inductance. At

the frequencies to be used, the inductance of the leads is significant and must be taken into account when deciding what total inductance is required to obtain the desired frequency of os-

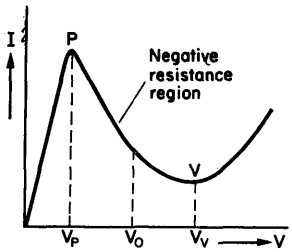



FIG. 9.22. Voltage–current characteristic of a typical tunnel diode. $V_p$ is the peak voltage and $V_v$ the valley voltage.

cillation. With the extra inductance added, the equivalent network may be redrawn as in Fig. 9.24 which is similar to the network of Fig. 9.2 from which the conditions for oscillation were

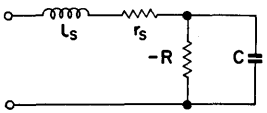



FIG. 9.23. Small signal equivalent network of a tunnel diode.

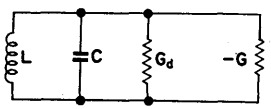



FIG. 9.24. Equivalent network of a tunnel diode, with external inductance, for the determination of the conditions for oscillation.

derived. $G_d$ is the effective shunt conductance across the tuned circuit; $G_d = 1/R_d = Cr/L$. By the same considerations as before, oscillations will build up if $G_d$ is less than $-G$.

*Design Considerations*

If the condition for build-up is satisfied, in the absence of an external load, the amplitude of oscillation will increase until the voltage peaks are carried into the region of positive resistance of the characteristic. In this condition the waveform will be highly distorted and a relatively low frequency of oscillation will result. If $L$ is decreased in value, the dynamic resistance of the tuned

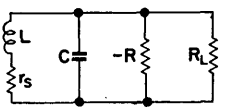



FIG. 9.25. Tunnel diode equivalent network with external load.

circuit is reduced and the load on the diode increased. This has the effect of reducing the amplitude of oscillation thus confining it to the negative resistance region. At the same time, the frequency increases as $L$ is further reduced until, when $L$ has a value which makes $G_d$ equal to $-G$, the maximum frequency of oscillation is obtained. This frequency, the cut-off frequency, is given by:

$$f_c = \frac{1}{2\pi RC}\sqrt{\left(\frac{R}{r_s} - 1\right)}, \tag{9.21}$$

where $R$ is the effective negative resistance, and $C$ and $r_s$ are the diode capacitance and series resistance. Instead of reducing $L$, the amplitude of oscillation may be restricted by an external load across the parallel tuned circuit which reduces the shunt conductance $G_d$. This may be represented by the approximate equivalent network of Fig. 9.25 provided that $R_L$ is much greater than $r_s$.

In practice, oscillations are confined to the negative resistance region by the adjustment of such a load and also by adjusting the d.c. bias across the diode.

Since as loading is increased, the amplitude of oscillation and the frequency decrease, the available output power may be

expressed as a function of frequency. This is done in the following equations given by McCann.[32]

Frequency of oscillation

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (\text{if} \quad R \gg r_s). \tag{9.22}$$

Load resistance

$$R_L = \frac{V_p'}{mI_p'}. \tag{9.23}$$

Power into load

$$P_L = \frac{mV_p'I_p'}{8}\ \mu\text{W} \tag{9.24}$$

where $V_p'$ and $I_p'$ are peak-to-peak values of voltage and current in millivolts and milliamps respectively. The symbol $m$ denotes the fraction of output appearing in $R_L$ and is given by:

$$m = 1 - \frac{2{\cdot}5\ V_p'}{300}\left(\frac{f}{f_e}\right)^2. \tag{9.25}$$

These expressions are not exact since they are based on an approximation for the negative resistance of the tunnel diode. They do, however, provide a useful first approach to the design of an oscillator which may be finally adjusted experimentally.

For germanium tunnel diodes, the maximum peak to peak voltage swing within the negative resistance region is $V_v - V_p$ equals about 300 mV, and this can only be supplied to a load at frequencies less than $0{\cdot}63f_c$. At frequencies greater than this, but less than $f_c$, the output voltage is reduced.

For gallium arsenide diodes, the maximum voltage swing is somewhat greater than 300 mV. Since for a given type the voltage swing differs little from one component to another, choice of diodes is limited to their available peak current, and hence the oscillatory power which they are capable of providing.

EXAMPLE. Consider an S.T.C. JK 30 A germanium tunnel diode for operation as a sinusoidal oscillator at 500 Mc/s. From the

manufacturer's data sheets, for a typical unit:

| | |
|---|---|
| Minimum lead inductance | $l_s = 1{\cdot}0$ mμH. |
| Junction capacitance | $c = 40$ pF. |
| Peak current | $I_p = 5{\cdot}0$ mA. |
| Valley current | $I_v = 0{\cdot}6$ mA. |
| Peak voltage | $V_p = 60$ mV. |
| Valley voltage | $V_v = 320$ mV. |
| Cut-off frequency | $f_c = 1100$ Mc/s. |

For maximum output power, the oscillatory voltage should extend over the full negative resistance region, giving a peak-to-

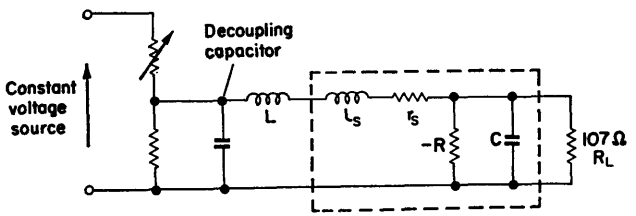



FIG. 9.26. Equivalent network of the tunnel diode oscillator. The variable resistor is used to set the operating bias point.

peak swing of 260 mV. The bias point should therefore be set at about 190 mV and made adjustable, as shown in Fig. 9.26.

From eqn. (9.25),

$$m = 1 - \frac{650}{300} \times \frac{25}{121} = 0{\cdot}55.$$

From eqn. (9.23),

$$R_L = \frac{260}{0{\cdot}55 \times 4{\cdot}4} = 107.$$

From eqn. (9.24),

$$P_L = \frac{0{\cdot}55 \times 260 \times 4{\cdot}4}{8} = 79\ \mu\text{W}.$$

An increase in the value of the load resistance would reduce loading on the diode and cause the voltage to swing into the positive resistance region. Oscillation would then take place in a relaxation mode. A decrease in the load resistance would result in a reduced output voltage, and hence a reduction in oscillatory power.

CHAPTER 10

# Waveform Generators

## Introduction

When the loop gain of an oscillator is very much greater than unity, the output waveform is not sinusoidal, but varies between two limits. Such non-linear oscillators have been examined by Van der Pol[33] and are known as relaxation oscillators.

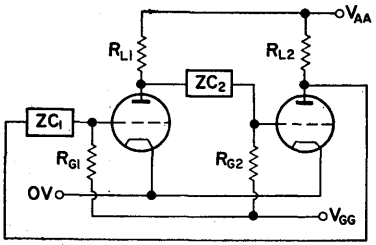



FIG. 10.1. Two-stage amplifier with output connected to input, thus forming a positive feedback system. The form taken by the coupling impedances, $Z_{c1}$ and $Z_{c2}$, determine the class of multivibrator.

The most important class of relaxation oscillators is the multivibrator family which may be divided into three main groups as follows:

(a) Astable multivibrators (A.M.V.), having no stable state.
(b) Monostable multivibrators (M.M.V. or flip-flop), having one stable state.
(c) Bistable multivibrators (B.M.V. or binary), having two stable states.

Each of these types can be considered as a two-stage amplifier with output connected to input, as shown in the circuit diagram of Fig. 10.1.

## 10.1. General Survey of the Three Types

*A.M.V.*

If the coupling impedances $Z_{C1}$ and $Z_{C2}$ are capacitors and $V_{GG} = 0$ the device is an astable multivibrator. Because of the

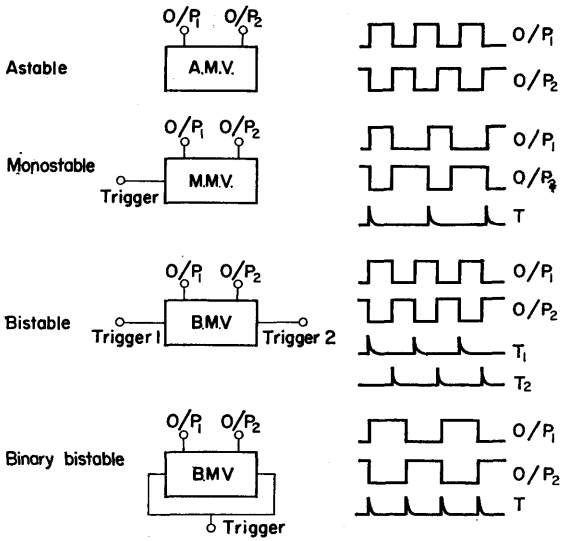



FIG. 10.2. Basic types of multivibrator.

a.c. coupling it has no stable state and will provide an output voltage of rectangular form, the duration of which is controlled by the time constants of the grid circuits.[34] Applications of the A.M.V. include:[35]

(a) *Timing oscillator.* The symmetrical A.M.V. can be used as a "clock generator" producing $X$ and $Y$ pulses, each anode providing one output. (See Fig. 10.2.)

(b) *Variable frequency oscillator.* The frequency of oscillation may be controlled electronically by varying $V_{GG}$ or mechanically, by changing component values in the grid network.
(c) *Frequency divider.* The A.M.V. can be readily synchronized to an input signal and used for counting down.
(d) *Harmonic generation.* Because of the rapid transitions of the waveform high order harmonics are generated.

*B.M.V.*

If the coupling impedances of Fig. 10.1 are resistive and $V_{GG}$ is taken to a negative value so that either valve may be held cut-off, the bistable conditions can be obtained.[36] It can be arranged that either valve is conducting, holding the other valve beyond cut-off, and such a stable state can be maintained indefinitely. To change the state of the device a trigger signal must be introduced. The B.M.V. is the most widely used type of multivibrator, and among its many applications there are:[36]

(a) *Counting.* As two successive input signals are necessary to restore the circuit to its original state, it may be used for counting by two.
(b) *Memory element.* The two alternative states of the B.M.V. may be designated "no" (or "0") and "yes" (or "1") and this facility is used in shift register circuits.

*M.M.V.*

If one coupling impedance is resistive and the other is capacitive the device will have one stable state. The valve with capacitive coupling is held "on", while the other valve is held "off" by the resistive coupling and negative $V_{GG}$. When triggered, a single output pulse is obtained, of duration determined by the grid time constant. The M.M.V. is commonly used for:

(a) *Pulse forming.* An input pulse can be transformed into a pulse of controlled duration and amplitude.

(b) *Counting.* The M.M.V., having once been triggered, is insensitive to further pulses until it reverts to its former state. This property makes the device useful as a counter.

(c) *Delay.* The trailing edge of the output waveform may be used to provide a pulse delayed from the input pulse. Since the duration of the output waveform can be controlled, as in the A.M.V., a variable delay is obtainable.

Although valves were the active elements originally employed in multivibrators, the transistor has proved to be more suitable in nearly all applications. Several hundred transistors may be operated for the same dissipation as one valve, and since both *npn* and *pnp* types are available, and direct coupling may be used, the transistor is more versatile than the valve. Most of the examples of this chapter are therefore devoted to the use of transistors.

## 10.2. Transistor Switching

### *Direct Coupling*

In Fig. 10.3a $T_1$ and $T_2$ are transistors having the typical characteristics of Fig. 10.3b. When $T_1$ is conducting $T_2$ is "off", because the bottoming voltage of $T_1$ is less than the conducting voltage of $T_2$.

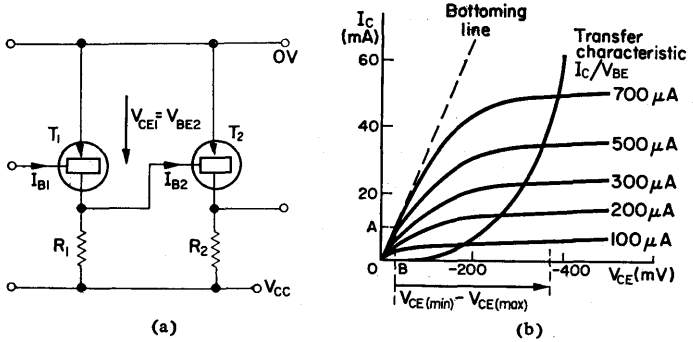



FIG. 10.3. Direct coupled transistors. When $T_1$ is conducting $T_2$ is off and vice-versa.

If the base of $T_1$ is supplied with a current of 1 mA, and if $V_{CC}/R_1 = 10$ mA, then $T_1$ will bottom at approximately 30 mV, which is less than the conducting value of $V_{BE}$ for $T_2$. If $I_{B1}$ becomes zero, the collector voltage of $T_1$ will try to approach $V_{CC}$, but the base of $T_2$ will hold the voltage to approximately 0·4 V. The major part of the current previously flowing into the collector of $T_1$ will now be flowing into the base of $T_2$. Thus,

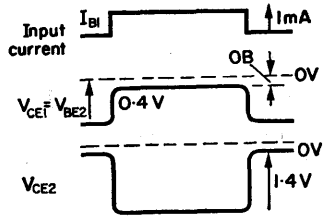



FIG. 10.4. Switching waveforms obtained from the transistors arranged as in Fig. 10.3.

although there is a transfer of current from $T_1$ to $T_2$, the voltage at the collector of $T_1$ changes by less than 0·4 V. This has been considered previously with respect to direct coupled amplifiers. The waveforms obtained are shown in Fig. 10.4.

*Resistor Coupling*

If a greater collector voltage swing is required, than is possible with direct coupling, the collector of $T_1$ may be connected to the base of $T_2$ by a resistor. Such a resistor reduces the base current $I_{B2}$ to a value that is sufficient to switch $T_2$, but does not cause excessive voltage drop in $R_1$. Thus, if $V_{BE2}$ and $I_{B2} \cdot R_1$ are neglected,

$$I_{B2} \doteq V_{CC}/R_B \quad \text{(see Fig. 10.5).} \tag{10.1}$$

Normally, $R_B$ is selected such that the transistor will just bottom. This gives a defined switching level of the order of 50 mV and ensures low power dissipation in the device. Referring to the characteristic curves of Fig. 10.6, if $R_C$ is 1 kΩ the drive current

required to bottom the transistor is approximately 120 μA. The value of base current required is a function of the collector current. If a larger collector resistor is used, the base current necessary for bottoming will be reduced.

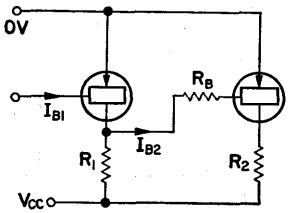



FIG. 10.5. Use of coupling resistor to allow a greater voltage swing at the collector of the first transistor.

*Saturated Operation*

The maximum current that can flow in the collector is the saturation current, and this occurs when $V_{CE}$ is a minimum ($\doteq$ 0 V). Thus, $I_{SAT} = V_{CC}/R_C$. For saturated operation, the

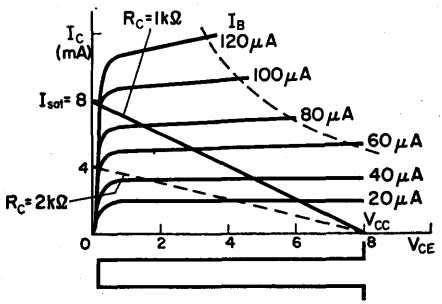



FIG. 10.6. Determination of the base current necessary to turn a transistor "on".

limits of the output waveform are: ($V_{CE} \doteq 0$ V, $I_C = I_{SAT}$) and ($V_{CE} \doteq V_{CC}$, $I_C = I_{CEO} \doteq 0$). The power dissipation, $P_C = I_C V_{CE}$ is small in either condition since in the first case $I_C \doteq 0$, and in the second case $V_{CE} \doteq 0$.

Collector current

$$I_C = I_{CE0} + h_{FE} \cdot I_B, \tag{10.2}$$

where $h_{FE}$ is the large signal s/c current gain. Thus, $I_B = I_{SAT}/h_{FE}$ gives the required value of base current for saturation. To ensure that saturation is attained the minimum value of $h_{FE}$ should be used.

## 10.3. Speed of Transistor Switching (Fig. 10.7)

When a transistor is switched on, for saturated operation it must pass through three different conditions:

(a) Transistor "off". The base–emitter junction is reverse biased and only leakage current flows in the collector circuit. $I_C = I_{CE0}$.
(b) Transistor in active region of operation. $I_C = I_{CE0} + h_{FE} \cdot I_B$.
(c) Transistor in saturated condition. $I_C = I_{SAT}$.

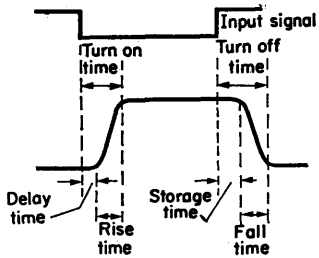



Fig. 10.7. Transistor switching sequence for a rectangular pulse input.

When the transistor is switched off the sequence is reversed, and the time taken to pass through these three conditions is the switching time.

The switching on sequence requires that a charge be put into the base, while when switching off the charge must be removed,

and the speed of operation is related to the time required to accomplish this. The increase in base current to provide such a charge, above that necessary for saturation, is called the overdrive current. Overdrive will decrease the turn-on time, but in general, will increase the turn-off time because of carrier storage. The use of overdrive makes provision for the spread in characteristics and ensures that transistors with the lowest current gain are bottomed.

To assist in charging and discharging the base, it is usual to shunt the coupling resistor with a *speed up* capacitor. This should be large enough to supply the required charge, but not so large as to slow down the switching time by requiring a large recharging period.

## 10.4. Transistor Bistable Multivibrator

Figure 10.8 represents the basic arrangement of a symmetrical, collector-to-base coupled circuit. It is required that, as a stable condition, when $T_1$ is conducting $T_2$ should be cut off.

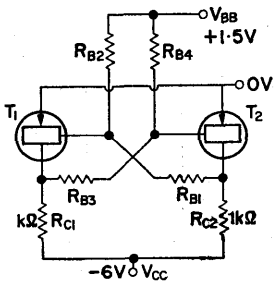



FIG. 10.8. Basic arrangement of a symmetrical collector-to-base coupled circuit.

The application of a positive trigger pulse to the base of $T_1$ drives it to cut off, and the resulting negative voltage transmitted from its collector to the base of $T_2$ causes that transistor to conduct. This state ($T_2$ conducting and $T_1$ cut off) is maintained until another trigger pulse is applied to the base of $T_2$.

*Design Considerations*

The choice of component values is to some extent a matter of compromise. Since the transistors are saturated when "on", the amplitude of the output voltage waveform is independent of the value of the collector resistor. The selection of this resistor is therefore a compromise between economy of current and speed of operation.

The speed-up capacitors are not essential for operation of the circuit, but should be used where small rise times are required. They should be chosen such that, with the coupling resistors, they form time constants equal to the transistor input circuit time constant, $r_{b'e} \cdot C_{in}$. A capacitor greater than this will decrease the rise time further, but tend to give an overshoot.

The use of a positive base supply $V_{BB}$ reduces the switching time out of the saturation condition. If the bias chain is of much greater resistance than the collector resistor, the collector voltage may be considered as being either at $V_{CC}$ or at 0 V, depending on whether the transistor is "off" or "on". Thus, when $T_1$ is conducting, $V_{C1} \doteqdot 0$, and the base voltage of $T_2$,

$$V_{B2} = V_{BB} \cdot \frac{R_4}{(R_3 + R_4)}, \tag{10.3}$$

which should be sufficient to hold $T_2$ cut off. When $T_1$ is cut off, $V_{C1} \doteqdot V_{CC}$ and $V_{B2}$ will be approximately $-0{\cdot}3$ V, causing $T_2$ to conduct.

*Choice of Transistor*

This is largely determined by the required speed of operation; if $f_1$ is the cut-off frequency of the transistor, then a speed of operation of the order of $f_1/10$ is possible.

*Design Steps*

1. Select values for the collector resistors, to provide the required saturation current.

2. Construct a load line on the characteristic curves, and determine the base current for saturation. Allow for 100% overdrive.
3. Calculate values for the coupling and bias resistors, and choose a suitable speed up capacitor.

DESIGN EXAMPLE 10.1

Required, a bistable multivibrator capable of operation up to 250 kc/s. A suitable transistor is the 2G301 having a cut-off frequency of 3–6 Mc/s. Let $V_{CC}$ be $-6$ V and $V_{BB} = +1{\cdot}5$ V.

Make $R_{C1} = R_{C2} = 1$ kΩ giving a saturation current of $V_{CC}/R_C = 6$ mA. If the load line is drawn in Fig. 10.6 it will be seen that a base current $I_B$ of 100 μA is required for saturation. Let the design figure be 200 μA to allow for transistors having low current gain (100% overdrive).

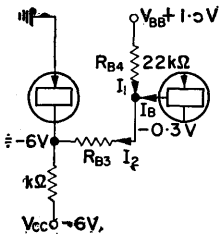



FIG. 10.9. Calculation of coupling resistance for Design Example 10.1.

*Bias resistors.* The positive bias supply must provide the leakage current $I_{CBO(max)}$ (= 60 μA, from the manufacturer's data). Thus,

$$R_{B2} = R_{B4} = \frac{V_{BB}}{I_{CBO(max)}} = \frac{1{\cdot}5\text{ V}}{60\ \mu\text{A}} = 25\text{ K}.$$

Let them have the preferred value of 22 kΩ.

*Coupling resistors.* When the base is forward biased, $R_{B4}$ passes current:

$$I_1 = 0{\cdot}08\text{ mA} \quad \text{(see Fig. 10.9)}.$$

But

$$I_2 = I_B + I_1 = 0{\cdot}28 \text{ mA}.$$

Therefore

$$R_{B3} = \frac{V_{CC}}{I_2} = \frac{6 \text{ V}}{0{\cdot}28 \text{ mA}} \doteqdot 21 \text{ k}\Omega.$$

This is a maximum value for $R_{B1}$ and $R_{B3}$ which may, with advantage be reduced to accommodate variations in voltage supply and resistor tolerances. Let the design value be 18 kΩ.

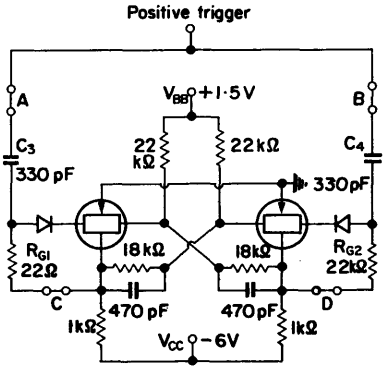



FIG. 10.10. Completed circuit of Design Example 10.1. The triggering arrangement provides binary operation.

*Speed-up capacitors.* The optimum value for speed-up capacitors can be calculated, but for the transistors chosen a value of 470 pF is indicated.

In Fig. 10.10 the completed circuit is drawn together with a suitable triggering arrangement.

## 10.5. TRIGGERING

To change the bistable from one state to the other, diode gating is usually employed. The "on" transistor forward biases the diode connected to its base, while the "off" transistor reverse biases its base diode. The former base will thus accept a positive pulse which switches it "off" and changes the state of the circuit.

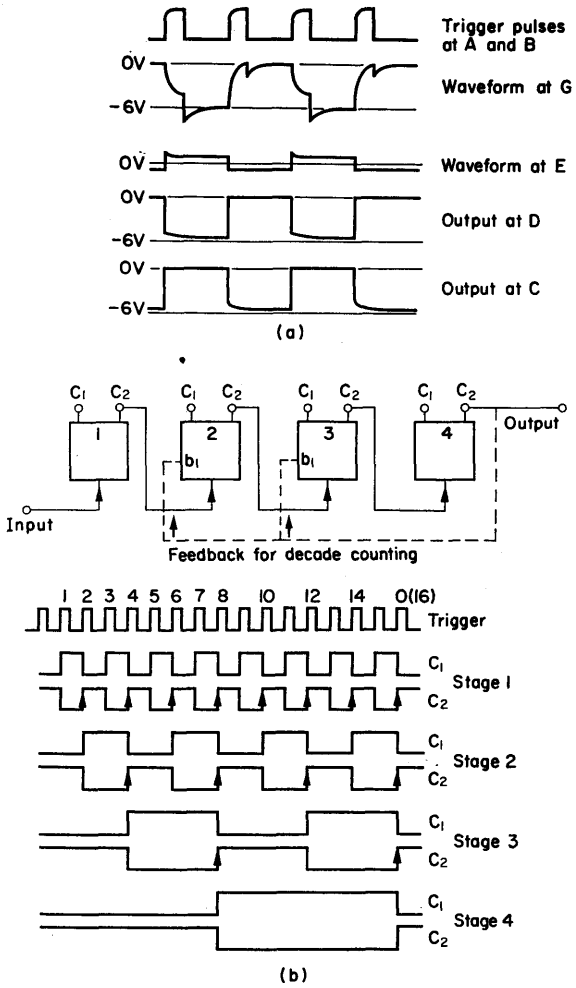



FIG 10.11. (a) Waveforms obtained when the circuit of Fig. 10.10 is operated as a binary element. (b) Connection of binary elements to form a four stage counter. This is basically a binary counter but application of feedback as shown transforms it into a decade counter.

In some applications, for instance shift registers, gating is controlled from another stage in which case the network is opened at $C$ and $D$. Other applications require two channels for input pulses. If the network is opened at $A$ and $B$, only the first pulse of a series on one channel will switch the device, unless the other channel is triggered. A series of waveforms obtained when the circuit is operated as a binary counter is drawn in Fig. 10.11 a.

*Input Capacitors $C_3$ and $C_4$*

These are required to switch off a transistor with a positive going trigger pulse. The selection of values is a compromise between ensuring operation and avoiding limitation of the repetition rate. They should be large enough to remove the base charge in the switching off sequence, but not so large that they are unable to discharge sufficiently before the arrival of the next triggering pulse.

## 10.6. Alternative Gating Methods

*Collector Triggering*

Referring to Fig. 10.12, with $T_1$ conducting, $D_1$ is reverse biased. Trigger pulses are therefore routed to the collector of

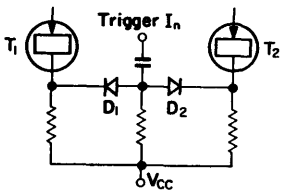



FIG. 10.12. Collector triggering for binary operation.

$T_2$ and from there to the base of $T_1$ via the cross-coupling network. This method has the advantage of only requiring one input capacitor, but a larger trigger pulse is necessary.

*Collector Triggering using a Transistor*

This method is frequently used for (DCTL) direct coupled logic circuits, and has the basic arrangement of Fig. 10.13. A negative voltage applied to the base of $T_3$ or $T_4$ will switch on the non-conducting transistor of the B.M.V. It will not, however, have any effect on the conducting transistor. The circuit may be modified to that of Fig. 10.14. Assume an initial condition of

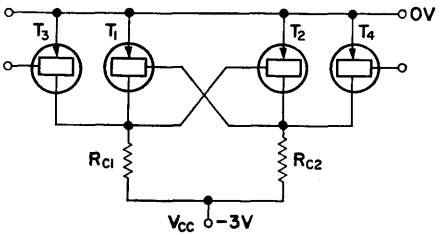



FIG. 10.13. Collector triggering using transistors. The trigger transistors are $T_3$ and $T_4$.

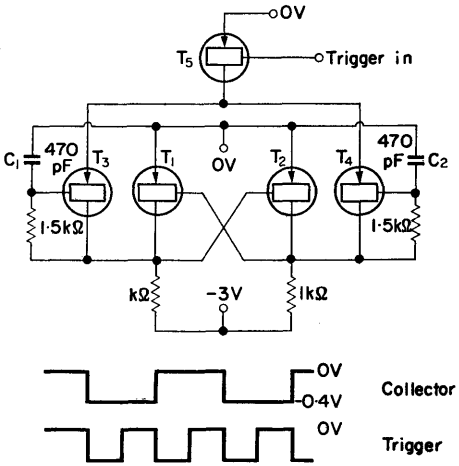



FIG. 10.14. Modification to the circuit of Fig. 10.13 to provide binary operation.

$T_1$ conducting and $T_2$ "off". Since $T_5$ is normally non-conducting, $C_1$ will only be charged to the bottoming voltage, but $C_2$ will be charged to the maximum collector voltage of $-0{\cdot}4$ V. The application of a trigger to the base of $T_5$, causing it to conduct, effectively connects the emitters of $T_3$ and $T_4$ to 0 V. Thus, the voltage on $C_2$ is applied between base and emitter of $T_4$, causing it to conduct, and this in turn switches off $T_1$ (and switches on $T_2$).

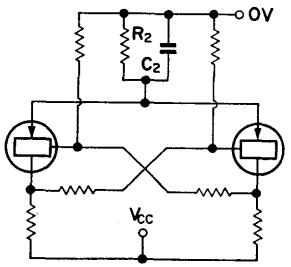



FIG. 10.15. Provision of base bias using emitter resistor $R_2$.

## 10.7. EMITTER COUPLED BISTABLE MULTIVIBRATOR

The positive base bias supply may be obtained by using a common emitter resistor, bypassed by a capacitor for high frequency currents, as shown in Fig. 10.15. To maintain the same conditions as in the previous example, $V_{CC}$ is increased by $-6$ to $-7{\cdot}5$ V. As the collector current is 6 mA,

$$R_E = \frac{V_{BB}}{I_E} = \frac{1{\cdot}5\text{ V}}{6\text{ mA}} = 250\,\Omega.$$

The switching time is of the order of 1 μsec, and the time constant $C_E R_E$ should be made at least 10 times greater than this. Let $C_E R_E = 10$ μsec. Then

$$C_E = 10^{-5}/250 = 4 \times 10^{-9}.\text{ Let it be } 0{\cdot}047\,\mu.$$

If the emitter resistor is not bypassed, emitter coupling can be used and one of the collector-to-base coupling networks removed.

The circuit then becomes that of Fig. 10.16. The regenerative loop consists of a common collector stage driving a common base stage, which is coupled back to the former by $R_{B3}$ and $R_{B4}$. The collector of $T_2$ is "free" since it does not enter directly into the feedback loop, and $R_{C2}$ can have any value provided that it is less than $R_{C1}$.

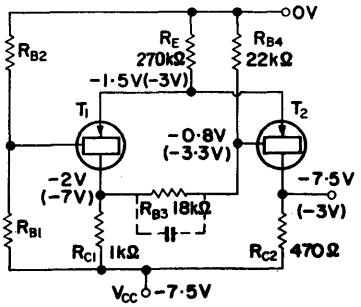



FIG. 10.16. Emitter coupled multivibrator. The voltages in brackets refer to the condition of $T_2$ conducting.

When $T_1$ is "on", $T_2$ is "off", because its base is positive with respect to the emitter voltage. When $T_2$ conducts it draws an increased current through $R_E$ cutting $T_1$ "off". The base voltage of $T_1$ will become more negative when $T_1$ is "off", because it will only be drawing leakage current. If it becomes $-2$ V, then its emitter should be approximately $-3$ V, to ensure that the emitter–base junction is reverse biased. Thus,

$$I_{E2} = \frac{V_E}{R_E} = \frac{3\text{ V}}{270} = 10\text{ mA}.$$

With $R_{C2} = 470\,\Omega$, the output voltage will vary between $-7{\cdot}5$ and $-3$ V. Such an arrangement has a loop gain less than unity at zero frequency and will not switch from one state to another. It will, in fact, perform as an amplifier with the output limiting at $-7{\cdot}5$ V (cut-off) or $-3$ V (conducting).

If $C$ is made sufficiently large, the circuit will have a gain which is greater than unity at high frequency, and will be switched by

relatively fast moving waveforms. The gain may also be increased by the use of a larger $R_{C1}$ or $R_E$. If $C$ is made 0·01 μF the device will perform effectively as a trigger circuit. Typical waveforms for the "switching" and "non-switching" states of this circuit are given in Fig. 10.17.

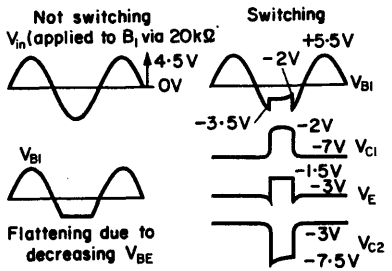



FIG. 10.17. Typical waveforms for the circuit of Fig. 10.16.

## 10.8. SYMMETRICAL TRIGGER B.M.V.

The symmetrical B.M.V. can also be used as a trigger device. To switch a transistor "on", the input voltage must be raised to a value that will produce conduction, and the reverse process is required for switching the transistor "off". The circuit of Fig. 10.18a can be triggered by the appropriate voltage at either

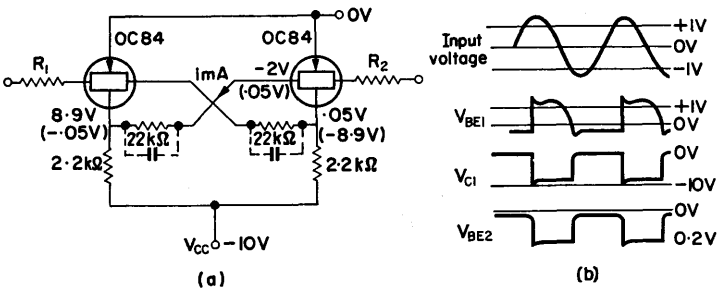



FIG. 10.18. Use of a symmetrical B.M.V. as a trigger device. The waveforms show the circuit being used to square a sine wave input.

base, i.e. −0·3 V to bring a transistor "on" and 0 V to switch "off". The waveforms obtained with a sinusoidal input are given in Fig. 10.18b.

## 10.9. Complementary Bistable Networks

If the *npn* and *pnp* transistors of Fig. 10.19 are biased correctly, the combination will have a current gain greater than unity with no signal inversion. It therefore has properties similar

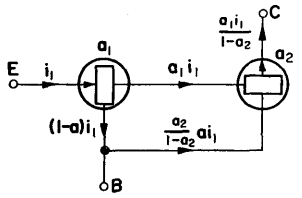



FIG. 10.19. Complementary pair to provide current gain without signal inversion.

to a point contact transistor, and is able to exhibit a negative resistance across its input terminals. The combination may be used in the form of Fig. 10.20. When $T_1$ is "off", $V_{C1} = -V$

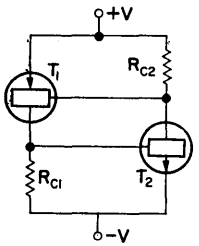



FIG. 10.20. Coupling of complementary device to provide a regenerative loop.

and $V_{BE2}$ is too small to turn $T_2$ "on". Both transistors are therefore "off". With $T_1$ "on", $V_{C1} \doteqdot +V$ and transistor $T_2$ also conducts.

A circuit employing this combination of transistors is given in Fig. 10.21. When the input voltage exceeds the reference voltage $V_R$, both transistors are switched on regeneratively. The emitter resistor $R_E$ draws current and $V_{E1}$ falls to approximately 3 V. A further fall in $V_{E1}$ will cause $T_1$ to start cutting off, which regeneratively switches off both transistors.

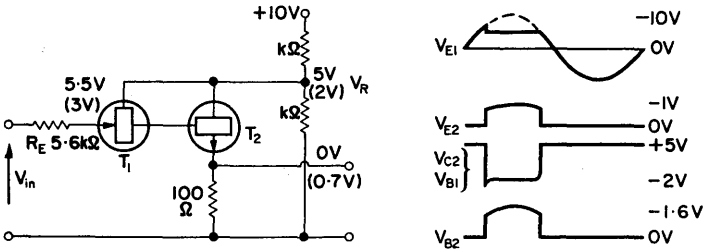



FIG. 10.21. Complementary bistable network. A square wave output is obtained from a sinusoidal input.

With such a network, a relatively large current pulse can be obtained from the emitter of $T_2$. Since the input circuit demands an increasing current as the voltage falls, it exhibits a negative resistance. The use of too large a value for $R_E$ can reduce the gain so much that the network will not switch.

## 10.10. THERMIONIC VALVE B.M.V.

### *Design Considerations*

The basic circuit is given in Fig. 10.22. For high frequency operation, the anode load resistors should be as small as possible, since when a valve is cut off the anode voltage rises on a time constant $C_A R_L$ where $C_A$ is the total anode capacitance. The cross-coupling networks must be so designed that each valve is held cut off when the other is conducting. Speed-up capacitors assist the switching action, as they do in the transistor circuit, and are usually in the range of 22–100 pF.

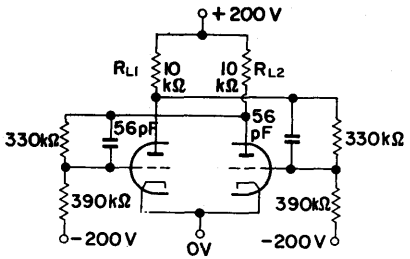



FIG. 10.22. Basic circuit of a thermionic valve B.M.V.

*Design Steps*

1. Plot a load line for the selected anode resistor, and determine the maximum and minimum voltages to which the anode is carried.
2. Calculate values for the coupling resistance chain such that, at the lower anode voltage (when one valve is conducting), the grid of the other valve is held well beyond the cut off voltage. Similarly, at the higher anode voltage (when the valve is cut off), the grid of the other valve is taken sufficiently positive to ensure full conduction.
3. Select a suitable speed-up capacitor.

*Choice of a Valve*

It is convenient to use a double triode for this application, and of the three mentioned in Chapter 1 the ECC82 (12AU7) is suitable. The high $g_m$ of an ECC81 could lead to instability, due to parasitic oscillation, whereas the low $g_m$ of an ECC83 is insufficient for this application.

DESIGN EXAMPLE 10.2

Required, a symmetrical bistable multivibrator, using an ECC82 valve from a $\pm 200$ V supply.

The load line for a 10 kΩ anode resistor is plotted on the characteristic curves drawn in Fig. 10.23. With the valve cut off the

anode voltage is at full h.t. When conducting, the valve draws grid current, holding the grid at 0 V, and the anode voltage is +90 V. Thus, the anode voltage swing is 110 V. In the "on" condition, the anode dissipation is 1·21 W which is well within the valve rating (2·5 W).

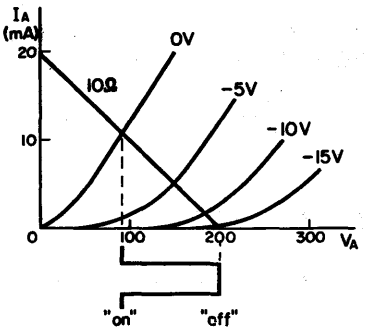



FIG. 10.23. Characteristic curves for an ECC82 with a 10 kΩ load line. The anode voltage swings through 110 V between cut-off and $V_{GK} = 0$.

*Coupling chain.* This is made of large value resistors, compared with $R_L$ so as not to limit the voltage swing of the anode. To ensure that the valve is cut off the grid voltage should be more negative than −20 V. The grid must be taken positive to ensure

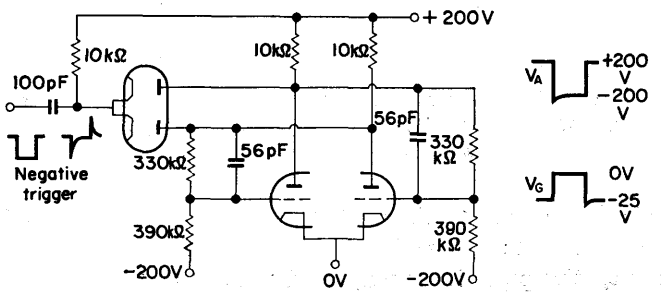



FIG. 10.24. Completed circuit of Design Example 10.2 with a suitable triggering arrangement.

that the valve is brought fully on. These conditions determine the ratio of $R_1$ and $R_2$, and are satisfied by $R_1 = 330\ \text{k}\Omega$ and $R_2 = 390\ \text{k}\Omega$. Using these values the grid is carried to $+10$ and $-43$ V in its two alternative states. The completed circuit, with a suitable triggering arrangement, given is in Fig. 10.24.

*Triggering.* Due to the connection between the cathodes and h.t., via the 10 kΩ resistor, the two diodes are so biased that only the one connected to the anode of the non-conducting valve passes the trigger signal. This is then routed to the grid of the "on" valve via the anode–grid coupling network.

*Alternative triggering and biasing.* The circuit diagram of Fig. 10.25 is an alternative arrangement in which a common cathode resistor is used to provide the necessary bias for the double

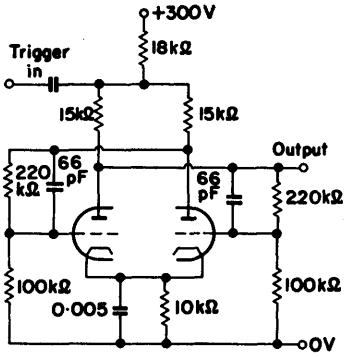



FIG. 10.25. Use of cathode bias to eliminate the need for a negative voltage supply, in a B.M.V. The triggering arrangement is suitable for a binary counter.

triode. This eliminates the need of a negative voltage supply. The common 18 kΩ anode resistor enables the binary to be triggered. The negative pulse is routed, via the anode of the "off" valve, to the grid of the "on" valve and causes it to switch off.

## 10.11. Cathode Coupled B.M.V.[40]

It is sometimes required that a voltage step (or a pulse) be generated when a voltage reaches a predetermined level. Such a facility is provided by the circuit of Fig. 10.26 which gives an output step of 30 V when the input voltage reaches 150 V. The valve used is an ECC81 operating from a supply voltage of +300 V.

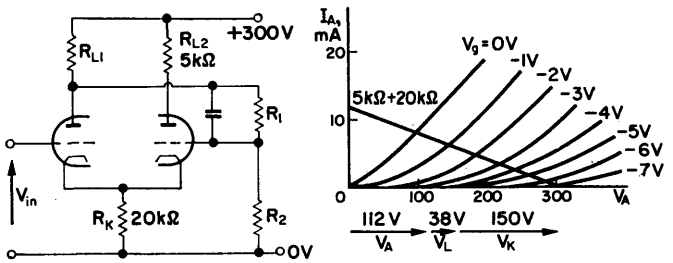



FIG. 10.26. Cathode coupled B.M.V. (Schmitt Trigger), switching at an input of 150 V.

### *Voltage at the Cathode*

It is required that $V_1$, which is initially cut off, should start conducting when $V_{IN}$ = 150 V. Thus, to make $V_{GK1} = -2$ V, the voltage at the cathode must be 152 V, and with this cathode voltage $V_2$ must be conducting. Let $R_K$ be 20 kΩ. Then, $I_{A2}$ = 152 V/20 kΩ = 7·6 mA which is the change in current which will occur when $V_2$ is switched "off". For an output voltage change greater than 30 V, $R_{L2}$ must be made 5 kΩ. The total load is therefore 25 kΩ and a load line for this value is plotted on the characteristic curves.

### *Voltage Divider $R_1R_2$*

The voltage divider $R_1R_2$ determines the cathode voltage of $V_2$ by cathode follower action. From the load line, for an $I_A$ of 7·6 mA, $V_{GK2} = -0{\cdot}5$ V, and thus $V_{G2} = 151{\cdot}5$ V. Since

$V_1$ is cut off, its anode voltage is +300 V, and $R_1$ should be approximately equal to $R_2$ to provide the required grid voltage. Let $R_1 = R_2 = 1\ \text{M}\Omega$.

### $V_1$ *Anode Resistor*

When $V_1$ conducts, the fall in anode voltage carries $G_2$ beyond cut off:

$$V_{G2} = \tfrac{1}{2}(V_K + V_{AK1}). \tag{10.4}$$

$V_2$ will start to conduct again when $V_{G2} \doteqdot V_K$, or, from eqn. (10.4), when $V_K = V_{AK1}$.

As $V_{IN}$ falls, $V_{AK1}$ increases until $V_{GK2}$ comes within the grid base. If $R_{L1}$ is made 5 kΩ, an input voltage of 150 V will switch $V_1$ "on", and the grid of $V_2$ will be carried to 131 V. This will cause $V_2$ to cut off. To bring $V_2$ back into conduction, $V_{IN}$ must be reduced to approximately 135 V, i.e. a "backlash" of 15 V

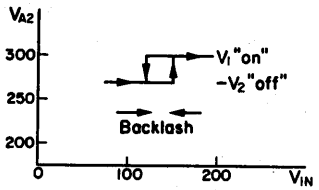



FIG. 10.27. Representation of "backlash" as a function of input voltage.

(see Fig. 10.27). If, however, $R_{L1} = 10\ \text{k}\Omega$, $V_{IN}$ must be reduced to 120 V to produce the changeover, and the backlash is 30 V. The choice of $R_{L1}$ is seen to be determined by the amount of backlash acceptable.

### *Reduction of Backlash*

Backlash may be reduced by using a smaller value for $R_{L1}$. If it is made too small, it is possible for the loop gain to fall below unity, and the switching action will cease. Alternatively, as

shown in Fig. 10.28, backlash may be reduced by amplifying the input signal. An amplifier of gain $A$ before the B.M.V. will reduce the backlash by the factor $1/A$.

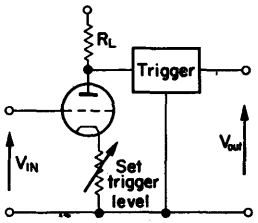



FIG. 10.28. Reduction of "backlash" by the use of an auxiliary amplifier. Backlash is reduced by the factor $1/A$ if the amplifier gain is $A$. The variable resistor permits adjustment of the voltage at which the device triggers.

## 10.12. MONOSTABLE MULTIVIBRATORS

Resistors and capacitors are the most common timing elements, although inductance–resistance timing is sometimes employed. The M.M.V. is used principally for pulse forming and delay generation.

### *Collector-to-Base Coupled M.M.V.*

Referring to Fig. 10.29, the connection from the collector of $T_1$ to the diode, via $R$, biases the diode such that it is "open" when $T_1$ is conducting, and "closed" when $T_2$ is conducting (i.e. when $T_1$ is cut off). Thus, a positive going waveform will be accepted to switch off $T_1$. When triggered, the positive excursion of the $T_2$ collector is transferred to the base of $T_1$ which is held beyond cut off while $C_B$ discharges through $R_{B1}$. When the base voltage of $T_1$ is sufficiently reduced, $T_1$ again conducts and $T_2$ is cut off until the arrival of the next trigger pulse. Timing is thus effected by the time constant $C_B R_{B1}$ and is largely independent of the supply voltages.

*Design Considerations*

With the initial conditions of $T_1$ conducting and $T_2$ cut off, the collector voltage of $T_2 = V_{CC}$ and the collector voltage of $T_1 \doteqdot 0$. If the value of $V_{BE1}$ for saturation is $V'_{BE1}$ ($\doteqdot 0{\cdot}3$ V), the voltage on the capacitor, $C_B \doteqdot V_{CC} - V'_{BE1}$. When the circuit is triggered, $T_2$ conducts and its collector voltage switches to the

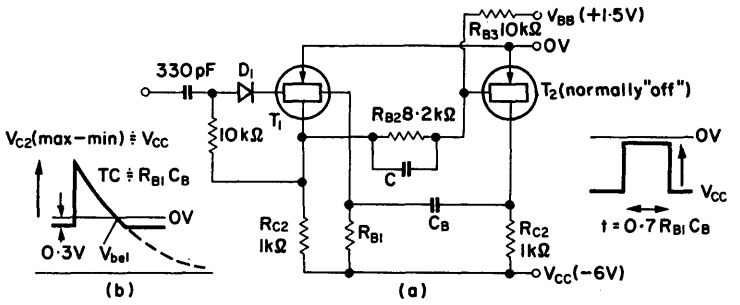



FIG. 10.29. Collector-to-base coupled M.M.V. A positive trigger at the input causes the generation of a rectangular pulse at the $T_2$ collector.

bottoming voltage, $V_{(\min)2}$, i.e. a voltage excursion of $V_{CC} - V_{(\min)2}$, and $T_1$ cuts off. The voltage on $C_B$ is therefore increased to:

$$V_{\max} = (V_{CC} - V'_{BE}) - (V_{CC} - V_{(\min)2})$$

$$= 2V_{CC} - V'_{BE} - V_{(\min)2}. \qquad (10.5)$$

$C_B$ now discharges through $R_{B1}$ according to the law:

$$v = V_{\max} \exp(-t/T), \qquad (10.6)$$

where $T$ is the time constant $C_B R_{B1}$. This is plotted in Fig. 10.29b. $T_1$ will start to conduct again when

$$v = V_{CC} - V''_{BE1}, \qquad (10.7)$$

where $V''_{BE1}$ is a little less negative than $V'_{BE}$ ($\doteqdot -0{\cdot}25$ V). Combining these three equations,

$$V_{CC} - V''_{BE1} = (2V_{CC} - V_{(\min)2} - V'_{BE}) \exp(-t/T). \tag{10.8}$$

Neglecting $V_{(\min)2}$, $V'_{BE}$ and $V''_{BE1}$,

$$\exp(-t/T) \doteqdot 0{\cdot}5.$$

Therefore

$$-t/T = \log_e 2,$$

and

$$t = 0{\cdot}7C_B R_{B1}. \tag{10.9}$$

If $R_{B1}$ is returned to $V'_{BB}$ instead of to $V_{CC}$, by similar considerations it may be shown that:

$$t/T = \log_e \frac{V_{CC} + V'_{BB}}{V_{CC}}. \tag{10.10}$$

Thus, the pulse length can be changed electrically by varying $V'_{BB}$.

The choice of collector resistor $R_C$ is a compromise. For economy of collector current and low collector dissipation a relatively large value is used. On the other hand a small value of $R_C$ is required, giving a small collector time constant for high speed operation. The use of a small $R_C$ has the added advantages, that it makes the circuit insensitive to external loading and also causes only a small voltage drop due to leakage current.

The positive base bias provided by $R_{B3}$ and $V_{BB}$ is only strictly necessary when operation over a wide temperature range is required.

*Design Steps*

1. Select values for $R_C$ and $V_{CC}$ which will permit the necessary rise and fall times of the output pulse.
2. Calculate the saturation current, i.e. the current which will cause $V_{CC}$ volts to be dropped across $R_C$.

3. Assume the minimum $h_{FE}$ for the selected transistor and determine the base current required for bottoming; choose values of $R_{B2}$ and $R_{B3}$ to provide this current.
4. Using eqn. (10.9), calculate values of $C_B$ and $R_{B1}$, to provide the required pulse length.

DESIGN EXAMPLE 10.3

Required, a monostable multivibrator to provide an output pulse of 5 μsec duration.

For this pulse length, rise and fall times of the order of 1 μsec are necessary, and typical values for $R_C$ and $V_{CC}$ are 1 kΩ and −6 V.

*Base resistors* $R_{B2}$, $R_{B3}$. $I_{sat} = V_{CC}/R_C = 6$ mA. With a minimum $h_{FE}$ of 20, $I_B = I_{sat}/h_{FE} = 300$ μA.

(a) If positive base bias is *not* used

$$R'_{B2} = 6\text{ V}/0{\cdot}3\text{ mA} = 20\text{ k}\Omega.$$

This represents a maximum value. Make $R'_{B2} = 15$ kΩ to allow for voltage variations.

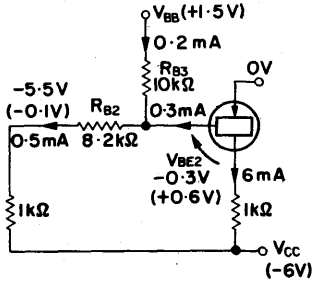



FIG. 10.30. Determination of the values of $R_{B2}$ and $R_{B3}$.

(b) If positive bias is used and $V_{BB} = 1{\cdot}5$ V, as shown in Fig. 10.30, let $R_{B3} = 10$ kΩ. Then, when $T_2$ is conducting the current in $R_{B3}$,

$$I_3 = \frac{1{\cdot}5\text{ V} + 0{\cdot}3\text{ V}}{10\text{ k}\Omega} = 0{\cdot}2\text{ mA}.$$

The current in $R_{B2}$,

$$I_2 = I_B + I_3 = 0{\cdot}5 \text{ mA}.$$

Voltage across $R_{B2}$,

$$V_1 = -V_{CC} - I_2 R_C + V_{BE}$$

$$= 6 - 0{\cdot}5 - 0{\cdot}3 \doteqdot 5 \text{ V}.$$

Thus,

$$R_{B2} = \frac{V_1}{I_2} = \frac{5 \text{ V}}{0{\cdot}5 \text{ mA}} = 10 \text{ k}\Omega.$$

Again to allow for voltage variations, let $R_{B2}$ have the preferred value of 8·2 kΩ. When $T_1$ is conducting its collector voltage $V'_{C1} = -0{\cdot}1$ V. Thus,

$$V_{BE2} = V_{BB} - \frac{R_{B3}}{R_{B2} + R_{B3}} (V_{BB} - V'_{C1})$$

$$= 1{\cdot}5 \text{ V} - 0{\cdot}9 \text{ V} = +0{\cdot}6 \text{ V}.$$

The base–emitter junction of $T_2$ is suitably reverse biased.

*Timing network* $C_B R_{B1}$. In small transistors the maximum base current is of the order of 1 mA.

Thus, the minimum value of $R_{B1} = V_{CC}/I_{B(\max)} = 6 \text{ V}/1 \text{ mA}$. Let $R_{B1}$ be the preferred value of 5·6 kΩ.

From eqn. (10.9),

$$C_B = \frac{t}{0{\cdot}7 R_{B1}} \doteqdot \frac{5 \times 10^{-6}}{4 \times 10^3} = 1250 \text{ pF}.$$

## 10.13. The Direct Coupled M.M.V. (Fig. 10.31)

*Operation*

In the stable state $T_2$, bottomed by the current in $R_B$, is conducting. A negative trigger pulse on the base of $T_3$ causes a reduction of the negative collector voltage of $T_3$ and $T_1$. This

change is transferred to the base of $T_2$ via $C_B$, which is charged to $V_{CC} - V'_{BE}$.

$T_2$ is thus cut off and held off for a period determined by the time constant $R_BC_B$.

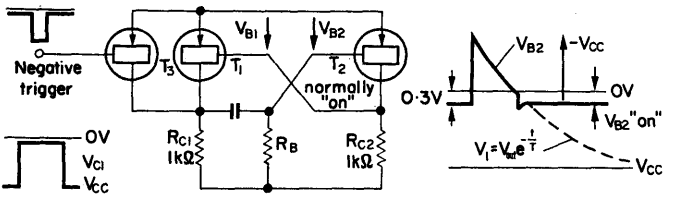



FIG. 10.31. The direct coupled M.M.V.

The exponential discharge of $C_B$ is terminated, and $T_2$ switches "on" when $V_{B2} \doteqdot -0{\cdot}25$ V. As in the previous example, it can be shown that

$$t = T \log_e \frac{2V_{CC} - V'_{BE}}{V_{CC} - V''_{BE}}, \tag{10.11}$$

and for $V_{CC} \gg V'_{BE}$,

$$t = 0{\cdot}7C_BR_B. \tag{10.12}$$

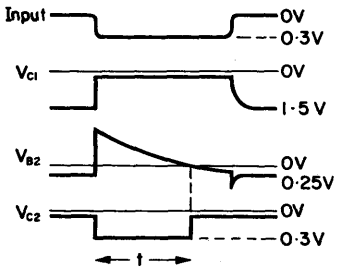



FIG. 10.32. Waveforms obtained from the circuit of Fig. 10.31.

EXAMPLE. Using an MA 240 transistor with $R_B = 10$ kΩ and $C_B = 1000$ pF, $T = 10^{-5}$ sec.

The waveforms obtained from such an arrangement are given in Fig. 10.32. Substituting values in eqn. (10.11) yields:

$$t = 10^{-5} \times 0{\cdot}78 \doteqdot 8 \ \mu\text{sec}.$$

*Collector saturation voltage.* The specification for the MA240 requires that, for $I_C = 2$ mA and $I_B = 0{\cdot}3$ mA, the saturation collector voltage should not exceed 70 mV. It is typically 40 mV.

*Base bias resistor* $R_B$. This should be small enough to allow $T_2$ to bottom.

If $R_{C2} = 1$ kΩ and $V_{CC} = -1{\cdot}5$ V, $I_{C(sat)} = 1{\cdot}5$ mA.

For a minimum $h_{FE} = 15$, $I_{B(sat)} = 1{\cdot}5$ mA/15 $= 0{\cdot}1$ mA.

Making $R_B = 10$ kΩ gives $I_B = 0{\cdot}12$ mA. If $I_{C(sat)}$ is increased (by making $R_{C2} = 500\,\Omega$, for instance), 10 kΩ will be too high a value for $R_B$, and the circuit will have no stable state, but will oscillate. Thus, as with all transistor monostable multivibrators, to provide large variations in pulse width $C_B$ must be varied and not $R_B$.

## 10.14. ASYMMETRICAL M.M.V.

The circuit of Fig. 10.33 represents an asymmetrical monostable multivibrator. In its normal state $T_1$ is "on", and $V_{E1} \doteqdot +0{\cdot}3$ V. The current $I_1 \doteqdot V_{EE}/R_{E1}$ is sufficient to ensure that $V_{C1}$ holds $T_2$ "off".

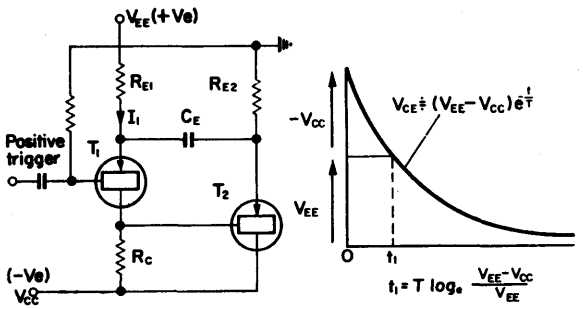



FIG. 10.33. Asymmetrical M.M.V. Because of the emitter coupling $T_2$ has a "free" collector.

The application of a positive trigger causes a reduction in $I_1$, and the resulting change in $V_{C1}$ allows $T_2$ to start conducting. The $T_2$ emitter therefore goes negative and, since $C_E$ cannot charge instantaneously, the emitter of $T_1$ is also taken negative. $T_1$ regeneratively switches off, and $T_2$ bottoms. In this fully switched state the emitters of both transistors are at approximately $V_{CC}$ volts and the voltage across $R_{E1}$ is $V_{EE} - V_{CC}$ (where $V_{CC}$ is negative for *pnp* transistors).

$C_E$ now starts to charge through $R_{E1}$ and when the charge reaches $V_{CC}$ volts, $T_1$ starts to conduct. $T_1$ then switches on regeneratively and $T_2$ switches off again.

## 10.15. ASTABLE MULTIVIBRATORS

The A.M.V. is a free running multivibrator which produces rectangular pulses at a predetermined repetition frequency. It may therefore be used as the basic timing circuit for sweep generators, counters, etc. Figure 10.34 represents a symmetrical

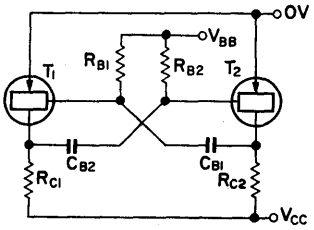



FIG. 10.34. Symmetrical A.M.V.

collector-to-base coupled circuit, having an operation as follows. Assume an initial condition of $T_1$ conducting and $T_2$ cut off. $C_{B2}$ now charges through $R_{B2}$ carrying the base of $T_2$ negative until $T_2$ starts to conduct. The collector voltage of $T_2$ then begins to rise, carrying the $T_1$ base positive; $T_1$ regeneratively cuts off and $T_2$ bottoms. $C_{B1}$ now charges, the base of $T_1$ goes negative until $T_1$ conducts again and the cycle repeats.

*Design Considerations*

The way base voltage varies with time is indicated in Fig. 10.35,

$$v_B = (-V_{CC} - V_{BB} + V'_{BE}) \exp(-t/T) + V_{BB},$$

where conduction takes place when $V_B$ falls to approximately $-0{\cdot}3$ V. If $V_{BE}$ is small compared with $V_{CC}$ and $V_{BB}$, and this is usually the case, then:

$$V_{BB} = -(V_{CC} + V_{BB}) \exp(-t/T)$$

or

$$t = T \log_e \left(1 + \frac{V_{CC}}{V_{BB}}\right)$$

$$= C_B R_B \log_e 2 \quad (\text{if } V_{CC} = V_{BB}).$$

Therefore

$$t = 0{\cdot}7 C_B R_B. \tag{10.13}$$

The period for a symmetrical system is $2t_1 = 1{\cdot}4\, C_B R_B$.

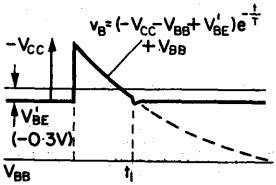



FIG. 10.35. Base waveform of the astable multivibrator.

*Design Steps*

1. Select suitable collector resistors and calculate the saturation current which will flow.
2. Using the minimum value of $h_{FE}$ for the type of transistor to be used, determine the minimum base current which will cause this saturation current.
3. Calculate the maximum value of $R_B$ to provide the necessary base current.
4. Using eqn. (10.13) evaluate $C_B$.

DESIGN EXAMPLE 10.4

Required, an astable multivibrator having a period of 0·1 msec. (i.e. a P.R.F. of 10 kc/s), using a $-1{\cdot}5$ V supply voltage. Let the transistor chosen be an MA 240 with a quoted minimum $h_{FE}$ of 15. Make the collector resistors 2·2 kΩ.

Collector saturation current

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{1{\cdot}5\text{ V}}{2{\cdot}2\text{ k}\Omega} = 0{\cdot}68\text{ mA}.$$

Minimum base current

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{h_{FE(\text{min})}} = \frac{0{\cdot}68\text{ mA}}{15} = 45\ \mu\text{A}.$$

The transistor will conduct when $V''_{BE} = -0{\cdot}3$ V.
Thus,

$$R_{B(\text{max})} = \frac{V_{CC} - V''_{BE}}{I_{B(\text{min})}} = \frac{1{\cdot}5 - 0{\cdot}3\text{ V}}{45\ \mu\text{A}} = 27\text{ k}\Omega.$$

This is the maximum value. Let the design value be 22 kΩ, to ensure saturation.

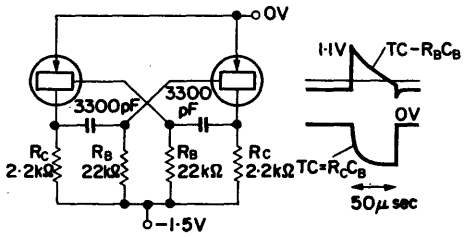



FIG. 10.36. Completed circuit of Design Example 10.4.

$$\text{Half period} = 0{\cdot}7C_BR_B = 50\ \mu\text{sec}.$$

Therefore

$$C_B = \frac{5 \times 10^{-5}}{0{\cdot}7 \times 22 \times 10^3} = 3300\text{ pF}.$$

The completed circuit is given in Fig. 10.36.

The collector waveform, obtained from this circuit, can be made more rectangular by the use of smaller collector resistors, thus reducing the time constant $R_C C_B$. Alternatively use may be made of the Darlington connection shown in Fig. 10.37. This connection gives a current gain of $(h_{FE})^2$, which, when substituted in the above calculations, leads to a bigger $R_B$ and smaller $C_B$. The $R_C C_B$ time constant is thus reduced.

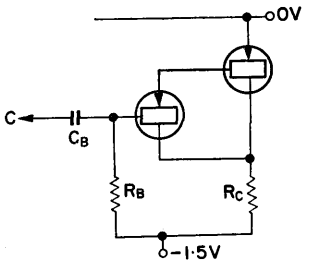



FIG. 10.37. The use of the Darlington connection leads to a better collector waveform than that obtained from the network of Fig. 10.36.

## 10.16. EMITTER COUPLED A.M.V.

The circuit has the form of Fig. 10.38 and is similar to the previously described emitter coupled M.M.V. The output waveform can be obtained from a "free" collector, i.e. one which does not enter directly into the feedback loop.

### *Operation*

When $T_2$ starts conducting, the base of $T_1$ is taken positive by the full excursion of the $T_2$ collector voltage, i.e. 20 V. Since the base of $T_1$ was originally held at 2 V positive by the base current in $R_1$, $V_{B1}$ becomes +22 V and the emitter voltage is 2 V.

The emitter of $T_2$ is held at approximately 0 V, because the base is earthed, and the $T_1$ emitter voltage rises on a time con-

stant approximately $C_2R_3$ as $C_2$ charges to $+6$ V. The charging current, which is drawn from the emitter of $T_2$, falls off exponentially and consequently the collector current of $T_2$, is reduced causing the collector to become more negative.

This charge is transferred to the base of $T_1$ via $C_1$ (which has no effect on the timing). Thus the $T_1$ base and emitter voltages approach equality and when the base becomes sufficiently negative, with respect to the emitter, $T_1$ conducts. The resulting voltage produced across $R_3$ is transferred to the emitter of $T_2$ making $V_{E2} \doteqdot -3{\cdot}5$ V, and $T_2$ is cut off.

The collector voltage of $T_2$ therefore changes to $V_{CC}$ and this change is applied to the base of $T_1$, completing the regenerative loop.

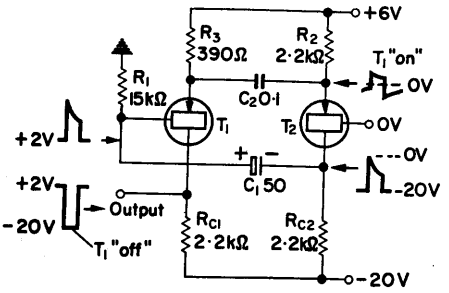



FIG. 10.38. Emitter coupled A.M.V. The free collector of this network provides a well-defined rectangular pulse.

The emitter voltage of $T_2$ now rises from $-3{\cdot}5$ V towards $+6$ V on the time constant $C_2R_2$. When the emitter reaches a slight positive voltage, $T_2$ conducts and the cycle repeats.

## 10.17. COMPLEMENTARY A.M.V.

The negative resistance arrangement of § 10.9 may be used with an $R$–$C$ network as an astable multivibrator, as shown in Fig. 10.39.

*Operation*

With both transistors "off" $V_{C2}$ is at 10 V, and point $A$ is held at 0 V by the diode. Point $B$ now rises towards 20 V on the time constant $C_1R_2$ until it is sufficiently positive, with respect to $V_{C2}$, to cause $T_1$ to conduct. This in turn brings $T_2$ into conduction. The current drawn by $T_2$ collector causes $V_{C2}$ to fall, and this

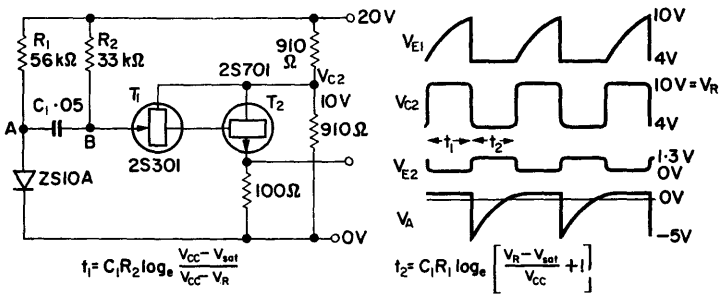



FIG. 10.39. Complementary astable multivibrator. $V_{sat}$ is the transistor saturation voltage.

fall is transferred to point $A$ via $T_1$ and $C_1$. Point $A$ is thus taken negative. It now rises towards 20 V on the time constant $C_1R_1$, but is caught at 0 V by the "catching" diode, and the transistors are switched "off".

## 10.18. DIFFERENTIATING AND INTEGRATING NETWORKS

It is frequently required that the rectangular waveform obtained from an A.M.V. be used to provide a narrow pulse at either its leading or trailing edge, or both. This may be accomplished by the simple "differentiating" network of Fig. 10.40. Since $C_d$ cannot charge instantaneously the leading edge of the input waveform appears across $R_d$. The capacitor $C_d$ now charges on the time constant $R_dC_d$, and the voltage across $R_d$ falls exponentially on the same time constant. After a time

$4C_dR_d$, the voltage across the resistor is approximately zero and remains thus until the arrival of the trailing edge. The sequence is then repeated in the opposite direction. The output from such a network, in response to an input rectangular waveform of duration $D$, is given in Fig. 10.41, and shows the effect of varying the time constant $C_dR_d$.

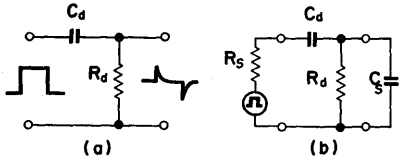



FIG. 10.40. Simple "differentiating" network.

In practice, the driving circuit will have some resistance $R_s$ and the resistor $R_d$ will be shunted by a capacitance $C_s$, e.g. the input capacitance of an amplifier to which the network is connected. The effective circuit is therefore that of Fig. 10.40b. The leading edge of the output waveform now rises on the time constant

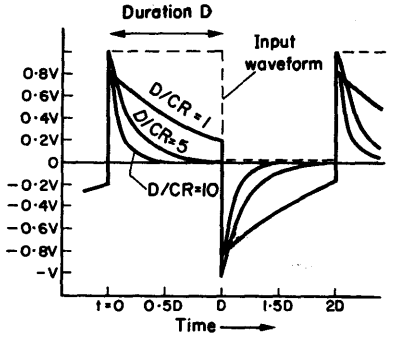



FIG. 10.41. Response of simple "differentiating" network to a rectangular waveform.

$R_sC_s$, but as this may be made very small, rise times of the order of a fraction of a microsecond are possible, provided that the rise time of the input waveform leading edge is faster than this.

The presence of $C_s$ also causes a reduction in the amplitude of the output signal. Thus,

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{C_d}{C_s + C_d}. \tag{10.14}$$

The output from a simple "differentiating" circuit is seen to be a positive "spike", synchronous with the positive-going leading edge of a rectangular input waveform, and a negative "spike" synchronous with the negative going trailing edge. These spikes may be squared-off and unwanted spikes removed by the use of limiter circuits.

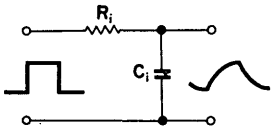



FIG. 10.42. Simple "integrating" network.

Even when limited, the pulse is not rectangular. However, it can be made to approach the rectangular shape by the use of a small value of inductance in series with $R_d$. If $L$ is made equal to $\frac{1}{2}C_sR_d^2$, then the resulting resonant effect will produce a pulse which is broader at the top and which has a steeper trailing edge.

If, as in Fig. 10.42, the output is taken from across the capacitor instead of from the resistor, the network acts as an "integrator". In fact a true integration of a rectangular waveform is a triangular waveform, i.e. one in which the voltage rises and falls linearly with time. In the simple network shown, however, both rise and fall are exponential with a time constant $R_iC_i$.

## 10.19. LINEAR SWEEP GENERATORS

Figure 10.43 represents an ideal linear sweep waveform having the law $V = at$ for $t$ greater than 0. Such a waveform is required for time-bases and is also used in comparator circuits.

A simple way of providing a sweep voltage is to charge a capaci-

tor through a large resistor. The charge is, of course, exponential, as shown in Fig. 10.44, but if only the first part of the output waveform is used, then a reasonably linear rise is obtained. For

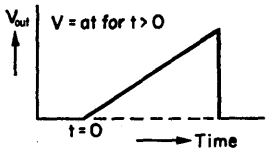



FIG. 10.43. Ideal linear sweep waveform.

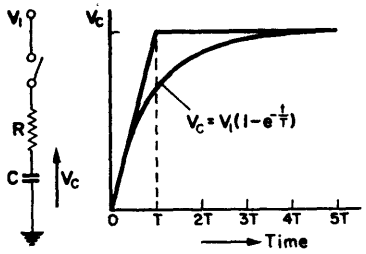



FIG. 10.44. Exponential rise in $V_C$ as a capacitor is charged through a resistor.

instance, if $v_C$ is allowed to rise to only 10% of the full voltage, the non-linearity is 5%:

$$v_C = V_1[1 - \exp(-t/T)].$$

$$v_C = \frac{V_1 t}{T}\left[1 - \frac{t}{2T} + \frac{t^2}{6T^2} \cdots\right]$$

$$= at\left[1 - \frac{t}{2T} + \frac{t^2}{6T^2} \cdots\right],$$

where $a = V_1/T$.

Thus, for small values of $t$, $v_C = at$ (as in Fig. 10.43).

At the end of the required sweep, the capacitor must be discharged, and this may be done by a transistor connected as in Fig. 10.45.

When non-conducting, i.e. during the sweep period, the transistor should be reverse biased. A silicon transistor is preferred to a germanium type in this application because of its low leakage current.

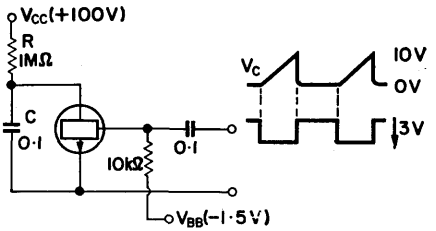



FIG. 10.45. Use of a transistor to discharge the capacitor of an $R$–$C$ sweep network.

## 10.20. USE OF A CONSTANT CURRENT GENERATOR (Fig. 10.46)

For a given supply voltage, the performance can be improved by charging the capacitor from a constant current generator instead of through a resistor. For a rise of 10 V in 10 msec,

$$\frac{dV}{dt} = \frac{I}{C} = 1000 \text{ V/sec.}$$

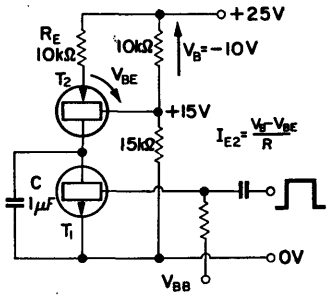



FIG. 10.46. Linear sweep generator. $T_2$ provides a constant current of approximately 1 mA.

Let $I$ be 1 mA, then $C = 1\ \mu F$.

$$I = \alpha I_E \doteqdot \frac{V_{B2}}{R_E}.$$

Therefore

$$R_E = 10\ k\Omega.$$

If $T_2$ is a silicon transistor, the resistance of the current source will be approximately $r_C$, i.e. several megohms.

## 10.21. Sawtooth Generator using Avalanche Switching

If the characteristics of a transistor are plotted for collector voltages greater than those normally used, they take the form of Fig. 10.47. With increasing collector voltage a region is reached where large collector currents result from very small changes in $V_C$. This region is known as the avalanche region and occurs at a collector voltage at which $h_{fb}$ tends to unity. The effect of

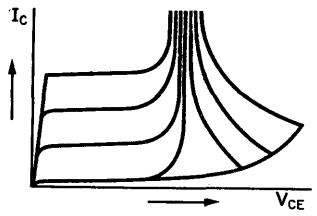



FIG. 10.47. Germanium alloy transistor characteristics showing avalanche breakdown region.

reverse biasing the base of the transistor is to hold off the breakdown point to a considerably greater voltage. Once breakdown is initiated, however, the voltage across the transistor falls to the lower value if the base resistor is sufficiently large. Figure 10.47 represents the breakdown characteristic of an OC44 transistor, and in Fig. 10.48 is drawn the circuit diagram of a sawtooth generator making use of this breakdown phenomenon.

*Sweep Amplitude*

The amplitude of the sweep obtained from such a circuit is effectively determined by the emitter voltage swing. The approximate range of this swing is between the breakdown voltages for (a) the collector–base junction with emitter open circuit, $V_{(BR)CBO}$, and (b) the collector–emitter with base open circuit, $V_{(BR)CEO}$. It is usually of the order of 20 V, and in this example is from 53 to 28 V.

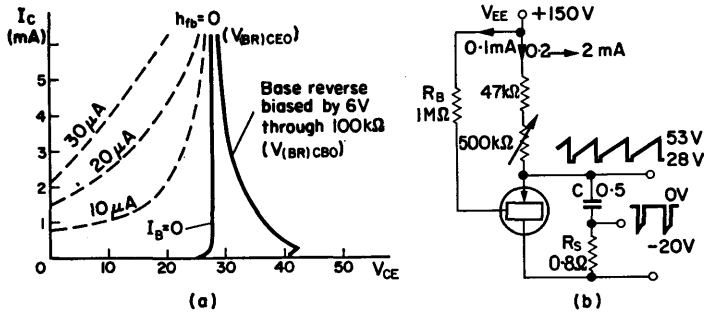



FIG. 10.48. Linear sawtooth generator using avalanche breakdown.

*Operation*

At the start of the sweep, the base of the transistor is held at $V_{(BR)CBO}$. The capacitor $C$ charges through the emitter resistor until the emitter–base junction becomes forward biased (i.e. the emitter reaches $V_{(BR)CBO}$). The voltage across the transistor then falls to $V_{(BR)CEO}$.

This transition is extremely rapid because of the negative resistance effect exhibited when the transistor current increases as the voltage decreases.

*Design Considerations*

*Supply voltage.* To obtain a linear sawtooth waveform the capacitor should be charged from a constant current source, and

the use of a high voltage and large series resistor is therefore indicated. The supply voltage should be at least 5 times the sawtooth amplitude.

For a germanium alloy transistor, providing a sawtooth amplitude of 20 V, let $V_{EE}$ be 150 V. The mean emitter voltage is approximately 40 V, and the voltage across the emitter resistor $V_R$ is 110 V.

*Sweep speed* $\mathrm{d}V/\mathrm{d}t$. For a maximum sweep speed of 20 V in 5 msec,

$$\frac{\mathrm{d}V}{\mathrm{d}t} = \frac{20}{5 \times 10^{-3}} = 4 \times 10^3 \text{ V/sec},$$

$Q = CV$, where $Q$ is the charge on the capacitor,

$$i = \frac{\mathrm{d}Q}{\mathrm{d}t} = C\frac{\mathrm{d}V}{\mathrm{d}t},$$

where $V$ is the voltage across $C$.

If $C = 0{\cdot}5\ \mu\text{F}$, $i = 0{\cdot}5 \times 10^{-6} \times 4 \times 10^3 = 2$ mA.

This current is supplied through the emitterresistor.

Thus,

$$i = V_R/R_E \quad \text{and} \quad R_E = \frac{110 \text{ V}}{2 \text{ mA}} = 55 \text{ k}\Omega.$$

Let $R_E$ be a 47 kΩ resistor in series with a 500 kΩ variable resistor. This will enable the sweep duration to the varied over the range 5–50 msec.

*Base resistor* $R_B$. This should be sufficiently large to limit the collector dissipation $P_C = I_B \,.\, V_{(BR)CBO}$. The dissipation is limited to 5 mW if $R_B = 1$ MΩ, so this is a suitable value.

*Peak emitter current.* A small value resistor $R_S$ in series with the capacitor serves to limit the peak emitter current which might otherwise damage the transistor. In this example it is made 68 Ω and the peak emitter current is limited to about 0·3 mA. A large negative-going pulse is obtainable across $R_S$, synchronous with the start of the sweep waveform.

## 10.22. Miller Timebase Generator

This widely used timebase generator is illustrated in Fig. 10.49 and makes use of an amplifier having signal inversion, to which negative feedback is applied. It is in fact the integrating network previously considered in Chapter 7.

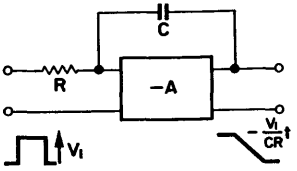



FIG. 10.49. Schematic diagram of a Miller integrator. The amplifier has signal inversion.

From eqn. (7.2),

$$\frac{v_{out}}{v_{in}} = \frac{\alpha A}{1 - A\beta} = -\frac{\alpha}{\beta} \cdot \frac{1}{1 - 1/A\beta},$$

where

$$\alpha = \frac{1}{1 + sCR} \quad \text{and} \quad \beta = \frac{sCR}{1 + sCR}.$$

Therefore

$$\frac{v_{out}(s)}{v_{in}(s)} = -\frac{1}{sCR} \cdot \frac{1}{1 - [(1 + sCR)/sCRA]}.$$

Rearranging, and for a step input of amplitude $V_1$,

$$v_{out}(s) = \frac{A}{CR(1 - A)} \cdot \frac{V_1}{s + [1/CR(1 - A)]}.$$

$$v_{out}(t) = AV_1\left[1 - \exp\left(\frac{-t}{CR(1 - A)}\right)\right]. \qquad (10.15)$$

The output voltage is thus the same as would be obtained from an amplifier fed from a capacitor $C(1 - A)$ in series with a resistor $R$, as shown in Fig. 10.50.

*Determination of non-linearity*

Expanding eqn. (10.15),

$$v_{out}(t) = \frac{AV_1 t}{CR(1-A)} \times \times \left[1 - \frac{1}{2}\frac{t}{CR(1-A)} - \frac{1}{6}\left(\frac{t}{CR(1-A)}\right)^2 - \ldots\right]. \tag{10.16}$$

Thus, for small $t$ the error is $\frac{1}{2}\frac{t}{CR(1-A)}$.

After one time constant, $t = CR$, the error is $50/(1-A)\%$, so for an error less than 1 % the amplifier gain $A$ should be greater than $-49$. Such a gain may readily be obtained from a single pentode valve, as shown in Fig. 10.51.

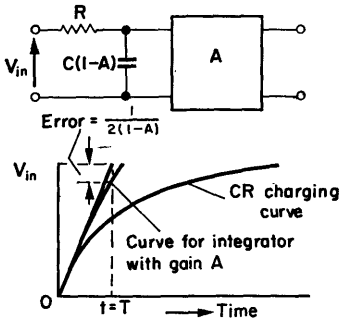



FIG. 10.50. Representation of Fig. 10.49 to show the effective increase in capacitance due to the amplifier gain.

*Operation*

In the initial condition, the valve is cut off by the negative bias on the suppressor grid. The control grid is slightly positive with respect to the cathode, and grid current flows. The anode voltage is at $V_{AA}$ so $C$ is charged to that value.

The circuit is triggered by a positive going rectangular waveform applied to the suppressor grid, the leading edge of which causes the anode to start conducting. The resulting fall in $v_A$ is transferred to the grid, via $C$, carrying it negative with respect to the cathode. This effect, which occurs at $t = 0$, is self-adjusting, the negative going excursions of $v_A$ being equal to that of $v_G$.

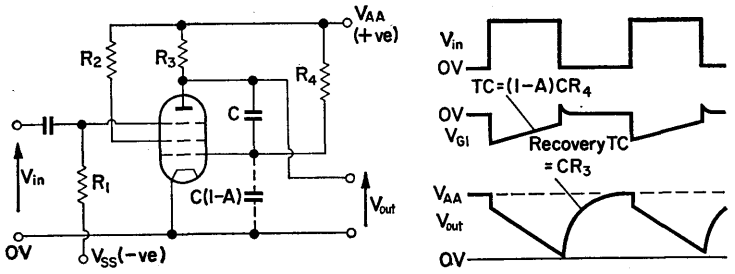



FIG. 10.51. Miller integrator. The gating waveform is applied to the suppressor grid, thus initiating "rundown".

The grid voltage takes up the necessary value to provide the required anode current. $C$ now starts to discharge through the resistor $R_4$ which demands a constant current,

$$I_R = \frac{V_{AA} - v_G}{R_4} \doteq V_{AA}/R_4.$$

Since $C$ is being discharged by this constant current the anode voltage must fall linearly. Thus,

$$Q = CV, \quad \text{so} \quad i = \frac{\mathrm{d}v_A}{\mathrm{d}t} C,$$

and the rate of change of anode voltage,

$$\frac{\mathrm{d}v_A}{\mathrm{d}t} = -\frac{i}{C} = -\frac{V_{AA}}{R_4}\frac{1}{C} \text{ volts/sec}, \qquad (10.17)$$

which is seen to be independent of the valve characteristics.

The time base is terminated by the arrival of the trailing edge of the gating waveform, which cuts the anode off. The anode voltage $v_A$ immediately rises and this rise, transferred through $C$, brings the grid voltage to zero where it is clamped by grid current. $C$ now charges on the recovery time constant $CR_3$, restoring the system to its initial state.

Alternatively, the circuit may be considered as an integrator of the form of Fig. 10.50. Using eqn. (10.16),

$$v_A(t) = \frac{AV_{AA}t}{CR_4(1-A)}\left[1 - \frac{1}{2}\frac{t}{CR_4(1-A)} \cdots\right], \tag{10.18}$$

where $A$ is the gain of the pentode, and will have a negative sign to indicate signal inversion. For a large $A$ the error terms may be neglected, and when this expression is differentiated, eqn. (10.17) is obtained.

## 10.23. Transistor Miller Timebase Generator

Consider an amplifier with low input resistance, and having a transfer impedance $Z_t = v_{out}/i_{in}$, connected as in Fig. 10.52. From eqn. (7.21), the forward voltage transfer function,

$$\frac{v_{out}(s)}{v_{in}(s)} = -\frac{Z_2}{Z_1}\frac{1}{1 - Z_2/Z_t}$$

$$= -\frac{1}{sCR}\frac{1}{1 - 1/sCZ_t}$$

$$= \frac{1}{CR}\frac{1}{s - 1/CZ_t},$$

$$\frac{v_{out}(t)}{v_{in}(t)} = \frac{Z_t}{R}[1 - \exp(t/CZ_t)], \tag{10.19}$$

where $Z_t$ is a negative quantity for negative feedback. Expanding eqn. (10.19) and for an input step of $V_1$ volts,

$$v_{out}(t) = -\frac{V_1 Z_t}{R}\left[\frac{t}{CZ_t} + \frac{1}{2}\left(\frac{t}{CZ_t}\right)^2 + \frac{1}{6}\left(\frac{t}{CZ_t}\right)^3 + \cdots\right]$$

$$= -\frac{V_1 t}{CR}\left[1 + \frac{1}{2}\left(\frac{t}{CZ_t}\right) + \frac{1}{6}\left(\frac{t}{CZ_t}\right)^2 + \cdots\right].$$

Thus, for an error less than 1% at $t = CR$, $50R/Z_t < 1$.

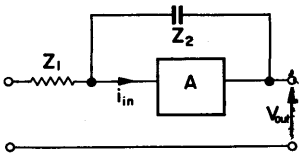



FIG. 10.52. Amplifier with transfer impedance $Z_t$ connected as a Miller timebase generator.

*Design Considerations*

The operation of the basic circuit, drawn in Fig. 10.53, is similar to that of the valve circuit. During the sweep period the capacitor is charged through $R$ and the recovery is on the time constant $CR_C$.

*Constant Current*

Ideally, it is required to maintain a constant current out of the capacitor. Since $V_{BE}$ does not change by more than a fraction of a volt the voltage across $R$, and hence the current through it, is effectively constant.

Thus,

$$I_R = V_{CC}/R. \qquad (10.20)$$

Not all this current is drawn from $C$, however, because of the base current which flows, but the circuit is designed so that $i_B$ forms only a small part of $I_R$.

*Output Voltage*

The output waveform varies between 0 V (transistor saturated), and $V_{CC}$ volts (transistor cut-off). Thus maximum current flows through $R_C$ with the transistor saturated

$$I_{max} = V_{cc}/R_C. \tag{10.21}$$

Using the values of Fig. 10.53,

$$I_{max} = 20\text{ V}/4\text{ k}\Omega = 5\text{ mA}.$$

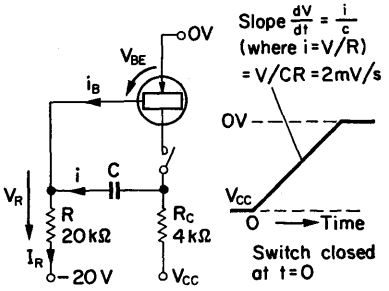



FIG. 10.53. Basic circuit of a transistor Miller timebase generator

While the time base is running $C$ requires an additional 1 mA, so the saturation current to be supplied from the transistor is 6 mA.

*Base Current*

The maximum base current

$$i_B = \frac{I_{C(sat)}}{h_{FE}} = \frac{6\text{ mA}}{80} \doteqdot 75\ \mu\text{A}. \tag{10.22}$$

At the end of the sweep $i_C$ is thus reduced by 75 μA, i.e. an error of 7·5%.

*Design Steps*

1. Using eqn. (10.21) select a value for $R_C$ to provide several milliamps maximum current.
2. Calculate the base current required for saturation.
3. Make $R$ of such value that the percentage of the current through it, provided by $i_B$, equals the acceptable percentage error by which the current may deviate.
4. Select $C$ to give the required sweep time constant and check that the recovery time constant $CR_C$ is acceptable.
5. Arrange suitable switching circuitry.

DESIGN EXAMPLE 10.5

Required, a timebase waveform of 20 V amplitude, 10 msec duration, and 10 msec recovery. The waveform is to have a linearity tolerance of 5%. Since the sweep amplitude is to be 20 V this value is chosen for $V_{CC}$.

*Collector resistor* $R_C$. To ensure a current of several milliamps, so that the full current gain $h_{FE}$ of the transistor is used and a low output resistance is obtained, let $R_C = 4\ \text{k}\Omega$.

*Base current*. For an $h_{FE}$ of 80,

$$i_{B(\max)} = \frac{20\ \text{V}}{4\ \text{k}\Omega} \times \frac{1}{80} = 60\ \mu\text{A}.$$

*Resistor* $R$. For 5% error, $I_R$ should be 20 times $i_{B(\max)}$ ($\doteq 1$ mA). Therefore

$$R = V_{CC}/I_R = \frac{20\ \text{V}}{1\ \text{mA}} = 20\ \text{k}\Omega.$$

*Capacitor*.

$$\frac{dV}{dt} = \frac{20\ \text{V}}{10\ \text{msec}} = 2000\ \text{V/sec} = \frac{V}{CR}.$$

$$C = \frac{V}{R}\frac{dt}{dV} = \frac{20\ \text{V}}{2 \times 10^3 \times 20 \times 10^3} = 0{\cdot}5\ \mu\text{F}.$$

*Recovery time.* The recovery time constant $CR_C = 0{\cdot}5 \times 10^{-6} \times 4 \times 10^3 = 2$ msec. The capacitor will thus be able to charge 20 V in 10 msec and the specification is met.

*Gating.* In the final circuit of Fig. 10.54, $T_2$ is used as a switch. It acts as a common base stage and does not change the current gain appreciably.

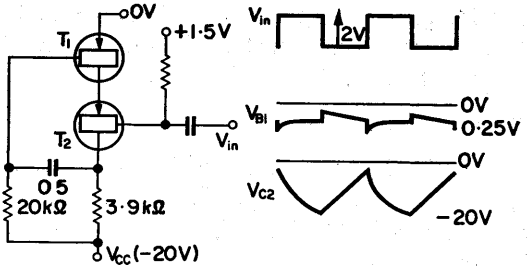



FIG. 10.54. Completed circuit of Design Example 10.5. Gating is effected by $T_2$.

## 10.24. REDUCTION OF RECOVERY TIME

The recovery time, which equals $5CR_C$, can be reduced by decreasing either $R_C$ or $C$. Reduction of $R_C$ requires an increase in base current which will reduce linearity. Alternatively, a reduc-

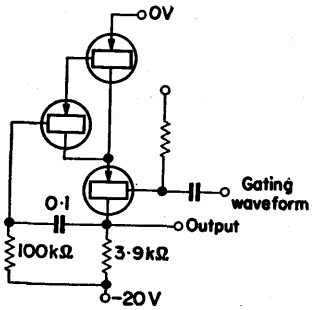



FIG. 10.55. Use of Darlington connection to reduce recovery time.

tion in $C$ necessitates a larger value for $R$ and again linearity is reduced. A solution is to make use of the Darlington connection which increases the current gain to approximately $(h_{FE})^2$. The base current is then reduced by $(h_{FE}^{-1})$ permitting $R$ to be increased without a reduction in linearity. The circuit is drawn in Fig. 10.55.

If $R = 100\ \text{k}\Omega$ for a 10 msec sweep duration $C = 1\ \mu\text{F}$, and the recovery time, $5CR_C = 2$ msec. This arrangement will provide a linearity at least 10 times better than in the previous example.

CHAPTER 11

# Some General Design Considerations

IN THIS chapter consideration is given to some general aspects of electronic design practice which are applicable to all the preceding design chapters. Subjects dealt with include the factors influencing the choice of resistors and capacitors, and the design centre rating system for thermionic valves. The chapter is concluded with some notes on screening and earths.

## 11.1. RESISTORS[42]

The main characteristics to be considered in selecting a resistor for a specific application are size, wattage rating, stability and tolerance. There are in addition, noise, maximum operating voltage, frequency range, and temperature and voltage coefficients, each of which may also be of importance in special cases.

Resistors may be divided into two groups, high stability and general purpose. The high stability group includes cracked carbon, wirewound and metal film resistors, while the general purpose component is usually of carbon composition construction.

### *Wattage Rating*

This specifies the maximum amount of power which may be dissipated in a component without excessive rise in temperature, and is usually stated for operation in an ambient temperature up to 40°C. Where the ambient temperature is in excess of this figure, the component should be derated in accordance with the manufacturers derating curves. Typically, a component rated at

40°C might have its maximum permissible dissipation reduced by 50% when used in an ambient of 70°C. It is good design practice to operate carbon resistors at 60% of their rated value.

*Stability*

This is an indication of the ability of a resistor to retain its stated value during a reasonable period of storage and also throughout its useful life.

*Tolerance*

Stated as a percentage of the resistance of the component, this indicates the maximum and minimum values which may be expected of a component having a given nominal resistance. The most common tolerances are ±20, ±10 and ±5% and a designer should anticipate that the majority of resistors will have values which lie close to the two limits. Components having 5% tolerance are normally only used in critical positions. In semi-critical positions such as anode, screen and bias resistors 10% tolerance may be used, while 20% components should only be employed as grid resistors or in other non-critical positions.

*Preferred Value*

Resistors are manufactured in a range of preferred values such that any resistor plus its tolerance is approximately equal in value to the next larger resistor minus its tolerance. The preferred values given in Table 11.1 are in accordance with both the American R.M.A. and British Standard specifications.

TABLE 11.1 PREFERRED RESISTOR VALUES

| | | | | |
|---|---|---|---|---|
| 10** | 16 | 27 | 43 | 68** |
| 11 | 18* | 30 | 47** | 75 |
| 12* | 20 | 33** | 51 | 82* |
| 13 | 22** | 36 | 56* | 91 |
| 15** | 24 | 39* | 62 | 100** |

Resistors are commonly available in multiples of ten of the stated values, between 10 Ω and 10 MΩ. The complete list of Table 11.1 is available in 5% components. Those marked with one asterisk are supplied in 5 and 10% tolerances, while those with two asterisks are obtainable in 5, 10 and 20%.

## 11.2. Resistor Types

### *Carbon Composition*

These are the cheapest resistors available and hence the most widely used. American types are available in ratings of ¼, ½, 1, 2, 4 and 5 W, while British types include ratings of $\frac{1}{10}$, ¼, ½, 1 and 2½ W. Stability generally is poor and the resistance may change several percent during lengthy periods of storage, and as much as 10% throughout the normal life of the resistor. In addition to thermal agitation noise which is present in all resistive elements, the composition resistor generates extra noise when current is flowing through it. This fact is only of serious importance in such specialized applications as are found, for instance, in the medical-electronic field where requirements often couple high gain with low noise.

### *Cracked Carbon*

Where a resistor of greater stability is required the cracked carbon type is employed. In normal use changes in resistance rarely exceed 2%, and such resistors are extensively used in the analogue computing field. Standard tolerances are ±1 and ±5% and wattage ratings are available from $\frac{1}{10}$ up to 2 W.

### *Wirewound Resistors*

These are manufactured with either ordinary or non-inductive windings and are used where even greater stability is desired, or where it is necessary to dissipate more power than is possible with carbon resistors. The load of a cathode follower circuit is

a typical application. Due to its type of construction the maximum value normally encountered is of the order of 50 kΩ. Wirewound resistors operate with high surface temperatures and should be sited so as to ensure adequate ventilation and to avoid damage to adjacent components.

## 11.3. CAPACITORS[43]

Capacitors are characterized by their stability, tolerance, working voltage, dielectric absorption, leakage current, insulation resistance and power factor. The first two of these characteristics have the same significance, referred to the value of capacitance, as was stated in § 11.1 for resistors.

### *Working Voltage*

This indicates the maximum voltage to which the capacitor should be subjected in normal use. It is commonly given for both d.c. and a.c. conditions and is valid over a given range of ambient temperatures. Where the stated ambient is exceeded, the working voltage should be suitably derated. Both working voltage and temperature influence the expected life of capacitor. In some types, operation at a temperature 10°C higher than the permitted maximum results in a reduction in life of 50%. Operation of capacitors at voltages much less than the stated maximum extends the life of the component significantly; an important consideration when designing equipment for which a high degree of reliability is required.

### *Dielectric Absorption*

If a fully charged capacitor is momentarily discharged, and then left open circuited, a further charge will build up in the component due to the energy absorbed by the dielectric during the charging process. The phenomenon is known as dielectric absorption and results in a reduction in capacitance as frequency is increased. It also introduces undesirable time lags in pulse and high speed switching circuits.

*Leakage Resistance*

When a capacitor is charged from a d.c. source and the source is then removed, the charge will not be held indefinitely but will leak away due to the flow of leakage currents. The effect is as if the capacitor was shunted by a resistance, and the time a given component takes to discharge to 36·8% of its initial charge is usually given as a $CR$ time constant. Leakage currents increase with temperature and are of significance where the capacitor is used to couple two points of different d.c. potential.

*Insulation Resistance*

This is an indication of the effective series resistance of a capacitor, and since it varies with capacitance, again a figure of ohms-farads is quoted. Where a capacitor is to be shunted by a high value resistance to provide a given time constant, the effect of insulation resistance on the resulting time constant should be considered. Such a requirement is often met in servomechanisms when stabilization is to be achieved by the use of passive networks.

*Power Factor*

When an alternating current flows in a capacitor the current leads the voltage by an angle somewhat less than the ideal 90°. The power factor of a component is the cosine of this phase angle and for a perfect capacitor equals zero. The power factor may also be defined as the ratio of power wasted per cycle to useful power per cycle. It is a function of applied voltage and determines the capacitor internal heating.

## 11.4. Capacitor Types

Capacitors are most conveniently grouped according to the dielectric used. Only the more commonly encountered types are here discussed.

*Ceramic*

These may be divided into two groups according to their permittivities and temperature coefficients. The first group having low permittivity, low loss and precise temperature coefficients find typical use in tuned circuits of radio receivers for temperature compensating purposes. Those having permittivities in excess of 500 generally provide less stability with changes in temperature, having higher losses and lower d.c. working voltage than the low permittivity types. They are only suitable for working with small a.c. voltages and are used mainly as r.f. bypass capacitors. Values up to 0·015 μF are commonly available with tolerances of ±20%.

*Mica*

Mica is a dielectric which provides high stability and low loss, and enables capacitors to be made with small capacitance tolerances. Working voltages are generally in excess of 300 V and insulation resistance is in the range 3000–6000 MΩ. Where good long-term stability is required silvered mica components may be used. They exhibit very small changes in value at frequencies up to several megacycles per second and are often used in v.h.f. intermediate frequency transformers. Mica capacitors have very low power factors and are available with 5, 10 and 20% tolerances and values ranging from 33 pF to 0·01 μF.

*Polystyrene*

The main advantages of the polystyrene capacitor are its low dielectric absorption, excellent power factor and very high insulation resistance which varies little with changes in temperature, enabling it to be used in long time constant circuits. This type of capacitor is extensively used in the analogue computing field. Its main disadvantage is the maximum temperature at which it should be used. This should not normally exceed 60°C.

*Polyester*

These are low cost components with high insulation resistance, but whose dielectric absorption is worse than that of polystyrene.

*Impregnated Paper*

These are relatively cheap general purpose capacitors providing high capacitance to volume ratios and capable of working at reasonably high d.c. voltages. Single units in tubular form are manufactured in values between 0·001 and 1·0 μF, generally having ±20% tolerance. For greater capacitance, a number of units are enclosed in a metal case and connected in parallel. Irrespective of the d.c. working voltages, the maximum a.c. working voltage for a single unit is normally about 300 V r.m.s. at 50 c/s. Insulation resistance varies according to the impregnant used and decreases with increasing temperature. For use for coupling between anode and grid, plastic impregnated capacitors are preferred to the wax impregnated type because of their higher resistance. The power factor of impregnated paper capacitors is in the range 0·005–0·01 at 1 kc/s and increases with frequency. Stability is normally of the order of 1–5%.

*Metallized Paper*

The use of metallized paper results in a smaller component for a given capacitance, and has the advantage that dielectric punctures caused by the application of excessive voltages are self-healing. Insulation resistance, however, is much less than that of impregnated paper types and for this reason they are not used for coupling purposes. They are, however, commonly used for decoupling h.f. and i.f. circuits where the main requirement is that of low impedance. The power factor of a metallized paper capacitor is about 0·02 at 1 kc/s and capacitance stability is normally between 5 and 10%.

*Electrolytic Capacitors*

These have a higher capacitance-volume ratio than any other capacitor, particularly at low working voltages, but they may only be used in circuit positions where they are subjected to substantially direct voltage. The capacitors must be connected correctly with regard to polarity and are extensively used as a.f. bypass and smoothing components. When used for smoothing in power supply circuits, care must be taken to ensure that not only is the maximum ripple voltage not exceeded, but also that the d.c. voltage plus peak ripple voltage is less than the voltage rating of the component. The maximum rated voltage for electrolytic capacitors rarely exceeds 500 V and is commonly made much less; 6 and 12 V ratings are readily available. When operated at the stated working voltage, leakage current is fairly high and increases with temperature. The operation of normal type electrolytic capacitors in high ambient temperatures and in the presence of large a.c. voltages tends to reduce their service life. These conditions should therefore be avoided in the interests of reliability. Where high ambient temperatures are expected tantalum electrolytic capacitors may be employed. These generally have lower leakage current than the normal type and are extremely small. Ratings are available between 2·5 and 25 V which makes them suitable for use in transistor circuits. Electrolytic capacitors generally have very wide tolerances, $-20\% + 100\%$ being typical.

## 11.5. Valve Rating Systems

A thermionic valve has usually been designed for a specific application, and the limiting conditions under which it may be operated are stated in the maker's data sheets. Such data is provided to enable the equipment designer to obtain maximum service life for the valve when used in the application for which it is intended. There are various systems by which these limiting conditions may be stated and the two most often used are

the "absolute-maximum rating system" and the "design-centre rating system".

*Absolute Maximum System*

This system originated in the early days of the thermionic valve, when all power supplies were obtained from batteries, so that all supply voltages could only decrease with time and rarely exceed their original values. The limitations imposed by this system only take account of changes in operating conditions caused by the anticipated spread in valve characteristics. As the name implies, such limitations are absolute, and the designer should ensure that they are not exceeded under the worst conditions. He should therefore take account of possible supply voltage fluctuations, load changes, variations in environmental conditions and tolerances in component values, and for each limitation, establish some average design value which is less than the stated absolute maximum.

*Design Centre System*

The three types of power supply systems now most commonly in use are, a.c. and d.c. mains, storage battery with connected charger, and dry batteries. To take account of the expected voltage fluctuations from these various systems, and because of the danger of absolute ratings being treated as if they were design ratings, valve data sheets now generally list limiting conditions according to the design centre system. In this system, the valve manufacturer has selected limiting values such that, providing they are not exceeded, the normal variations in power supply voltages, environmental conditions, component values and loads, etc., will not cause the absolute ratings for that type of valve to be exceeded. It is assumed that good design practice is followed and that the valve is only used for the purpose for which it has been manufactured.

For both these systems the stated ratings are to some extent interdependent and care should be taken to ensure that in work-

ing at one maximum rating another rating is not automatically exceeded. It is, in fact, quite common for a single rating to determine the operating conditions of a valve.

## 11.6. General Recommendations

The subjects of valve rating systems and recommendations for the use of thermionic valves, have been treated in detail elsewhere.[44] A few of the more important considerations are set out below.

### *Supply and Heater Voltages*

Provided that design centre ratings have not been exceeded, equipment may be operated from power supplies whose voltages variations are limited to $\pm 10\%$. Where, however, such variations are encountered, and where mains transformer tappings are provided, it is good practice to make suitable adjustment so as to operate the valve heaters at a voltage or current as close to the nominal value as possible. Operation at the rated voltage or current leads to optimum valve life and performance. For indirectly heated valves with heaters connected in parallel, the heater voltage of individual valves should, in any case, be within $\pm 7\%$ of the rated voltage when the supply voltage is at its nominal value.

### *Valve Electrodes*

Valves should always be operated with a d.c. connection between each electrode and the cathode. For indirectly heated valves the electrode voltages quoted in the maker's data sheets are given with respect to the cathode.

### *The Cathode*

With the exception of certain rectifier valves, the voltage between cathode and heater should be kept low and generally

should not exceed 100 V. Where this voltage cannot be kept low, the resistance between heater and cathode should be kept as high as possible, i.e. a high value cathode resistor is indicated. However, from consideration of hum and heater-cathode leakage current, the cathode resistor should not normally be greater than 20 kΩ.

*The Control Grid*

The maximum permissible value of resistance between control grid and cathode is usually given in the maker's data sheets and this value should not be exceeded. The limit is imposed to prevent reverse grid current carrying the grid potential increasingly positive, thus causing increasing anode current and leading to the possible destruction of the valve. It is good design practice to keep the grid–cathode resistance as low as possible, and generally, with self-bias, 1 MΩ should be the maximum value used.

*The Screen Grid*

As the onset of control grid current is often determined by the screen grid voltage, in circuits where a low grid bias voltage is used, low screen grid voltages should be avoided. In some power output circuits it is common practice to connect the screen grid direct to h.t. provided that the screen dissipation is not exceeded. In the presence of large signals, however, the effect of a cathode resistor is reduced and a screen resistor then becomes necessary; one which drops the h.t. voltage by 20% is usually sufficient.

## 11.7. SCREENING[45]

When an electric current flows in a conductor electromagnetic energy is radiated, the magnitude of which is a function of the amplitude and frequency of the current. Any conductor situated within the radiated field will have some of this energy induced in it, and thus undesirable coupling between different parts of a circuit may result. It is sometimes possible to mitigate this effect

by arranging that equal and opposite self-cancelling voltages are induced. This is the principle which dictates that the conductors providing the alternating filament current to a valve should be twisted together, to avoid the pick up of hum voltages at mains frequency. The method is effective up to 5 kc/s, and the effectiveness depends to a large extent on the uniformness and tightness of the twist employed. The adequate separation of the component parts of a circuit from a radiating source will also reduce pick up, since, at a distance, the flux density will be reduced. Where however such methods are ineffective, an attempt must be made to contain the radiated field by means of a conducting screen, and the following notes are intended as a guidance to this end.

*Selection of Screening Materials*

The effectiveness of a conducting screen in reducing the energy of an electromagnetic wave is the result of two effects.

(a) Absorption loss as the wave passes through the conducting medium.

(b) Reflection loss occurring at each surface of discontinuity.

Both are frequency dependent and are also affected by the nature of the material. The provision of a screen should aim at causing the maximum overall loss to a radiated field, and the material chosen depends on whether the field is largely electric or magnetic.

In general, magnetic materials provide greater absorption loss to radiated electromagnetic energy, while good conductors, such as copper or aluminium, give more reflection loss. These latter materials make effective screens for electric fields, but their efficiency falls as frequency is increased. Aluminium is nevertheless commonly used for v.h.f. intermediate frequency transformer screening cans. In the presence of an alternating magnetic field, the screening efficiency of aluminium and copper falls as frequency decreases. At low (audio) frequencies, therefore, it is necessary to employ such high permeability metals as Mu-metal or Permalloy to provide satisfactory screening of magnetic fields.

*Screening of Cables*

This is mainly influenced by the impedance of the radiating source and the pick-up cable.

*High Impedance Radiators*

These are conductors having large series impedance (greater than 1 kΩ), in which h.f. voltages may be developed, with respect to earth, with very little current flowing. The radiation field is largely electric and can induce large h.f. voltages in adjacent high impedance circuits, but little current in low impedance circuits. A high impedance circuit is here intended to mean a circuit having a high termination impedance. A lead connected to the control grid of a valve may therefore be considered to be a high impedance circuit, and thus susceptible to such radiation. The use of copper braid screening is effective in preventing pick up from such a source, provided that the screen is at earth potential along its entire length. For short leads earthing at one end is usually sufficient, but at high frequencies and for long leads the screening should normally be earthed at more than one point.

*Low Impedance Radiators*

These are metallic conductors making a closed loop, which permits large currents to flow while developing little voltage. The fields resulting from such a source are largely magnetic and can induce large currents in low impedance circuits but little voltage in high impedance circuits. Conventional copper braiding is not effective in preventing magnetic coupling below 5 kc/s, but its effectiveness improves as frequency increases.

*Earths and Earth Loops*

Where, in a piece of electronic equipment, connections are made to earth at various points, currents may flow between such points, through the earth path. If these currents are at high fre-

quency, the earth loops so formed can act as low impedance radiators as defined above. The resulting fields, which are largely magnetic, can induce currents in low impedance circuits, physically close to earth, which are difficult to remove. For this reason, in high frequency equipment it is good practice to make earth connections at a single point.

The need for care in the use of multiple earths is not restricted to equipment operating at high frequencies. It is, for instance, of extreme importance in zero frequency (d.c.) amplifiers, in which requirements often couple high gain with low noise. In order to meet the low noise requirements, three different earths are commonly specified, signal earth, chassis earth and power earth. The first of these provides a reference for signal voltages and must therefore be kept "clean". Where it is necessary to make connection between the signal path and earth, for instance through a series *C–R* network for stabilization purposes, it is to signal earth that such connection is made. It is necessary that the chassis of an amplifier be held at earth potential for safety in handling, and also so that valve screening cans, which are connected to chassis, shall be effective as screens. A separate lead is therefore provided for earthing the chassis, and this too should be kept relatively free from noise. Since most noise arises from the power supplies, either in the form of h.t. ripple or in mains hum, the return path of h.t. power supplies is via a separate power earth connection. The three earths thus specified should not be "commoned" at the amplifier, but should be connected by separate leads to a single earth point at the power supply unit. This ensures that noise currents do not flow in the signal and chassis earths, giving rise to noise voltages at the amplifier output.

APPENDIX A

# Solutions of Simple Network Problems

## Basic Network Theorems[46,47]

### (a) Kirchhoff's Current Law (KCL)

The algebraic sum of currents flowing into a point (or node) is zero. Thus, in Fig. A.1,

$$i_1 + i_2 + i_3 = 0. \tag{A.1}$$

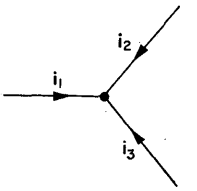



FIG. A.1. Kirchhoff's current law. $i_1 + i_2 + i_3 = 0$.

### (b) Kirchhoff's Voltage Law (KVL)

The sum of voltages around a closed loop is zero. Thus, in Fig. A.2,

$$v_1 + v_2 + v_3 = 0. \tag{A.2}$$

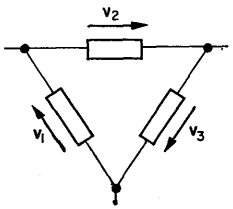



FIG. A.2. Kirchhoff's voltage law. The arrows indicate that the instantaneous voltage is measured from head to end. $v_1 + v_2 + v_3 = 0$.

EXAMPLE A.1. It is required to find the voltage across $R_3$ of Fig. A.3.

By KCL, the current flowing into node $A$ is equal to the current flowing out of it

$$i = i_1 + i_2; \tag{A.3}$$

and for node $B$,

$$i_2 = i_3. \tag{A.4}$$

From Ohm's law,

$$i_1 = \frac{v_1}{R_1}, \quad i_2 = \frac{v_1 - v_2}{R_2}, \quad i_3 = \frac{v_2}{R_3}.$$

Using conductances in place of resistances, eqns. (A.3) and (A.4) can be written as follows:

$$(G_1 + G_2)\, v_1 - G_2 v_2 = i \quad \text{(node } A\text{)}, \tag{A.5}$$

$$-G_2 v_1 + (G_2 + G_3)\, v_2 = 0 \quad \text{(node } B\text{)}. \tag{A.6}$$

These equations can be written down on inspection. The elements associated with $v_1$ are $G_1$ and $G_2$, and the coupling element with node $B$ is $G_2$.

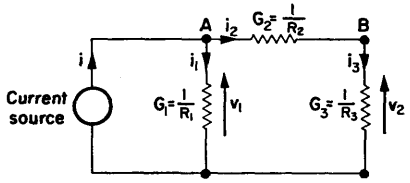



FIG. A.3. Network for example A.1. The elements are drawn as conductances for nodal analysis.

Similarly, for node $B$, at which the voltage is $v_2$, the elements are $G_2$ and $G_3$, and the coupling element is again $G_2$. In this case there is no current generator and the right-hand side of the equation is zero.

From the above equations, the voltages $v_1$ and $v_2$ can be found as functions of the input current. A simple method of solving these simultaneous equations is as follows.

The coefficients of the left-hand sides of the equations are set out as an array,

$$\begin{vmatrix} (G_1 + G_2) & -G_2 \\ -G_2 & (G_2 + G_3) \end{vmatrix}.$$

If the elements of this system are cross-multiplied, the *determinant* of the equations is obtained, provided that the product of the upper right and lower left terms is made negative.

Thus, the determinant

$$\Delta = (G_1 + G_2)(G_2 + G_3) - (-G_2)^2,$$
$$= (G_1G_2 + G_2G_3 + G_3G_1). \tag{A.7}$$

Replacing the left-hand column of the coefficient array with the right-hand sides of eqns. (A.5) and (A.6) the following array is obtained:

$$\begin{vmatrix} i & -G_2 \\ 0 & (G_2 + G_3) \end{vmatrix}.$$

Cross-multiplying,

$$\Delta_{v1} = (G_2 + G_3)\, i. \tag{A.8}$$

Similarly, if the right-hand side of the coefficient array is replaced by the right-hand sides of eqns. (A.5) and (A.6),

$$\begin{vmatrix} (G_1 + G_2) & i \\ -G_2 & 0 \end{vmatrix},$$

and the determinant is,

$$\Delta_{v2} = G_2 i. \tag{A.9}$$

Using eqns. (A.7), (A.8) and (A.9),

$$v_1 = \frac{\Delta_{v1}}{\Delta}$$
$$= \frac{(G_2 + G_3)\, i}{(G_1G_2 + G_2G_3 + G_3G_1)}. \tag{A.10}$$

$$v_2 = \frac{\Delta_{v2}}{\Delta}$$
$$= \frac{G_2 i}{(G_1G_2 + G_2G_3 + G_3G_1)}. \tag{A.11}$$

All the simultaneous equations in this book can be solved by this method which may be extended to deal with more complicated systems.[48] Since $v_1$ and $v_2$ are the voltages at the nodal points, eqns. (A.5) and (A.6) are the *nodal equations* and are formed by *nodal analysis*.

EXAMPLE A.2. Consider the network of Fig. A.4. If the dependent variables are assumed to be the loop or circuital currents $i_1$ and $i_2$, these can be determined by the application of KVL. The currents are drawn flowing in a clockwise direction to assist in the formalization of the equations. Thus,

$$(R_1 + R_2)\, i_1 - R_2 i_2 = v, \quad \text{for loop 1}, \tag{A.12}$$

$$-R_2 i_1 + (R_2 + R_3 + R_4)\, i_2 = 0, \quad \text{for loop 2}. \tag{A.13}$$

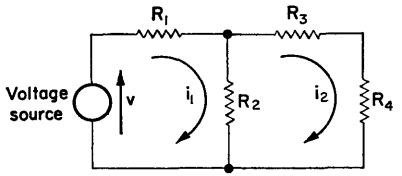



FIG. A.4. Network for example A.2. Loop currents $i_1$ and $i_2$ are drawn in a clockwise direction.

Proceeding as in the previous example, the coefficient array is

$$\begin{vmatrix} (R_1 + R_2) & -R_2 \\ -R_2 & (R_2 + R_3 + R_4) \end{vmatrix}$$

and the determinant is

$$\begin{aligned} \Delta &= (R_1 + R_2)(R_2 + R_3 + R_4) - (-R_2)^2 \\ &= (R_1R_2 + R_1R_3 + R_1R_4 + R_2R_3 + R_2R_4). \end{aligned} \tag{A.14}$$

$$\begin{vmatrix} v & -R_2 \\ 0 & (R_2 + R_3 + R_4) \end{vmatrix}$$

so that,

$$\Delta_{i1} = (R_2 + R_3 + R_4)\, v, \tag{A.15}$$

and,

$$i_1 = \frac{\Delta_{i1}}{\Delta} = \frac{(R_2 + R_3 + R_4)\, v}{R_1(R_2 + R_3 + R_4) + R_2(R_3 + R_4)}.$$

Also,

$$\begin{vmatrix} (R_1 + R_2) & v \\ -R_2 & 0 \end{vmatrix},$$

so that,

$$\Delta_{i2} = vR_2, \tag{A.16}$$

and,

$$i_2 = \frac{\Delta_{i2}}{\Delta} = \frac{vR_2}{R_1(R_2 + R_3 + R_4) + R_2(R_3 + R_4)}.$$

Equations (A.12) and (A.13) are *circuital equations* and are formed by *circuital analysis.*

APPENDIX B

# Application of the Laplace Transform

WHEN a network contains reactive as well as resistive elements, the equations are in integral–differential form. For the LCR circuit shown in Fig. B.1, the equation resulting from the application of Kirchhoff's voltage law is

$$v = Ri + \frac{1}{C}\int_0^t i\,dt + L\frac{di}{dt}. \tag{B.1}$$

By using the Laplace Transformation it is possible to transform the equation into an algebraic form, which can then be treated in same manner as the equations of Appendix A.

Equation (B.1) after transformation becomes,

$$\begin{aligned} v(s) &= Ri(s) + \frac{1}{sC}i(s) + sLi(s) \\ &= \left(R + \frac{1}{sC} + sL\right)i(s), \end{aligned} \tag{B.2}$$

where $v$ and $i$ are functions of the Laplace variable $s$ instead of time as is implied in eqn. (B.1). Integration is indicated by an $s$ in the denominator, and differentiation by an $s$ in the numerator. Thus in Fig. B.1 $R$, $C$ and $L$

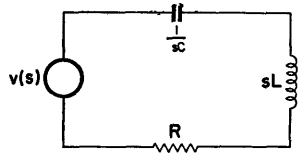



FIG. B.1. An $L$–$C$–$R$ circuit with transformed impedance.

can be represented by the transformed impedances $R$, $1/sC$ and $sL$. (If before the application of the voltage there is charge on the capacitor or current in the inductance, the representation is a little more complex and reference should be made to a standard work on network theory.[46,47])

Thus,

$$i(s) = \frac{v(s)}{R + (1/sC) + sL}. \tag{B.3}$$

If $v$ is a sinusoidal signal, which is the case for a frequency response measurement, the Laplace variable $s$ can be replaced by $j\omega$. The circuit current as a function of frequency is then,

$$i(j\omega) = \frac{v(j\omega)}{R + (1/j\omega C) + j\omega L}. \tag{B.4}$$

If it is required to determine the form of the output for a given input signal, the equation can be changed back into the time domain by using the inverse transforms given in Table B.1. This method is employed in § 3.9 to find the time response of a capacitively coupled amplifier.

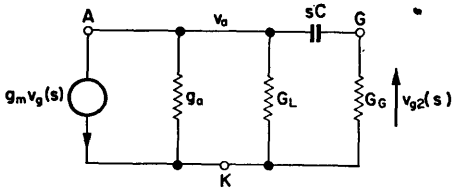



FIG. B.2. Transformed network for nodal analysis of the low frequency performance of a valve amplifier.

EXAMPLE B.1 Figure B.2 represents the anode network of a n amplifier It is required to find the frequency response and the output signal resulting from the application of a rectangular step of voltage to the input terminals of the amplifier.

The nodal equations are written down by inspection, using the method given in Appendix A:

$$(g_a + G_L + sC)\, v_a(s) - sCv_{g2}(s) = -g_m v_{g1}(s), \tag{B.5}$$

$$-sCv_a(s) + (G_G + sC)\, v_{g2}(s) = 0. \tag{B.6}$$

$$v_{g2}(s) = \frac{-g_m sCv_{g1}(s)}{(g_a + G_L + sC)(G_G + sC) - (sC)^2} \tag{B.7}$$

$$= \frac{-g_m}{(G_G + g_a + G_L)} \cdot \frac{1}{1 + [G_G(g_a + G_L)/(G_G + g_a + G_L)\, sC]}\, v_{g1}(s)$$

or

$$\frac{v_{g2}(s)}{v_{g1}(s)} = A_0 \frac{1}{1 + (1/sT_2)} \tag{3.6}$$

if the substitutions of § 3.5 are used.

TABLE B.1. LAPLACE TRANSFORM PAIRS

| | Function of time | Function of $s$ | |
|---|---|---|---|
| 1. | $1\ (t > 0)$ | $\frac{1}{s}$ | Step function of unit amplitude applied at time $t = 0$ |
| 2. | $V\ (t > 0)$ | $\frac{V}{s}$ | Step function of amplitude $V$ |
| 3. | $\exp(-at)$ | $\frac{1}{s + a}$ | |
| | | $\frac{1}{s} \quad \frac{1}{1 + (a/s)}$ | |
| 4. | $1 - \exp(-at)$ | $\frac{a}{s(s + a)}$ | |
| | | $\frac{1}{s} \quad \frac{1}{1 + (a/s)}$ | |

If the frequency response expression is required, the Laplace variable is replaced by $j\omega$.

Thus,

$$\frac{v_{g2}(j\omega)}{v_{g1}(j\omega)} = A_0 \frac{1}{1 + (1/j\omega T_2)}.$$

Since the Laplace transform of a rectangular step input of amplitude $V$ is $V/s$ (from Table B.1), the output as a function of $s$ is

$$v_{g2}(s) = A_0 \frac{1}{1 + (1/sT_2)} \cdot \frac{V}{s}. \tag{B.8}$$

By using transform pair 3 from Table B.1 the output response as a function of time can be obtained directly.

Thus,

$$v_{g2}(t) = A_0 \exp(-t/T_2)\ V. \tag{B.9}$$

The form of the response is shown graphically in Fig. 3.18.

APPENDIX C

# Symbols used in this book

British Standard Specification No. 3363, 1961, entitled "Letter symbols for light-current semi-conductor devices", makes recommendations for symbols to be used when describing transistor circuits. This system has been extended, in the same form, for use with thermionic valve circuits and is stated briefly below.

## Symbols

*a* or *A*, Anode
*g* or *G*, Grid
*k* or *K*, Cathode
*s* or *S*, Screen
} Thermionic valve

*c* or *C*, Collector
*b* or *B*, Base
*e* or *E*, Emitter
} Transistor

*v* or *V*, Voltage
*i* or *I*, Current
*P*, Power

$\left.\begin{matrix} i \\ v \end{matrix}\right\}$ with subscripts $\left\{\begin{matrix} c \\ b \\ e \end{matrix}\right\}$ or $\left\{\begin{matrix} a \\ g \\ k \end{matrix}\right\}$ represents the instantaneous value of a varying component.

$\left.\begin{matrix} i \\ v \end{matrix}\right\}$ with subscripts $\left\{\begin{matrix} C \\ B \\ E \end{matrix}\right\}$ or $\left\{\begin{matrix} A \\ G \\ K \end{matrix}\right\}$ represents the instantaneous total value.

$\left.\begin{matrix} I \\ V \end{matrix}\right\}$ with subscripts $\left\{\begin{matrix} c & a \\ b \text{ or } & g \\ e & k \end{matrix}\right\}$ represents the r.m.s. value of a varying component.

$\left.\begin{matrix} I \\ V \end{matrix}\right\}$ with subscripts $\left\{\begin{matrix} C & A \\ B \text{ or } & G \\ E & K \end{matrix}\right\}$ represents the d.c. or no-signal value. Maximum and minimum values are indicated by the use of subscripts (max) and (min).

## Electrical Parameters

| | *Device* | *Associated Circuit* |
|---|---|---|
| Resistance | $r$ | $R$ |
| Reactance | $x$ | $X$ |
| Impedance | $z$ | $Z$ |
| Admittance | $y$ | $Y$ |
| Conductance | $g$ | $G$ |
| Inductance | $l$ | $L$ |
| Capacitance | $c$ | $C$ |

## Double Subscripts

Where capital $V$ has two capital subscripts, this represents a voltage supply provided for the particular electrode of the device. For example $V_{CC}$ refers to a transistor collector supply voltage while $V_{GG}$ represents a voltage supply provided specifically for the grid of a thermionic valve. Where the two subscripts are different, the first subscript denotes the terminal at which the voltage is measured and the second subscript denotes the reference terminal. For example, $V_{BE}$ represents the d.c. or

no-signal voltage measured at the base, with respect to the emitter of a transistor. Other parameters may also be denoted by the use of double subscripts, as with $c_{gk}$ the capacitance which exists between the grid and cathode of a valve, or $r_{bb}$ the resistance between the actual base point and the base connector.

## Matrix Notation

The first subscript in the matrix notation for semiconductor devices identifies the element of the four-pole matrix. Thus,

*i* input
*o* output
*f* forward
*r* reverse

A second subscript is used to identify the circuit configuration:

*e* common emitter
*b* common base
*c* common collector

For example, using *h* parameters:

$h_{ib}(h_{11})$—The small signal value of the input impedance with the output short circuited to alternating current.

$h_{rb}(h_{12})$—The small signal value of the reverse voltage transfer ratio with the output voltage held constant.

$h_{fb}(h_{21}, \alpha)$, $h_{fe}(h'_{21}, \beta)$ The small signal forward current transfer ratio with the output short circuited to alternating current.

$h_{ob}(h_{22})$, $h_{oe}(h'_{22})$ The small signal value of the output admittance with the input open circuited to alternating current.

Static values of parameters are indicated by capital subscripts, e.g.,

$h_{FE}$ The static value of the forward current transfer ratio with the output voltage held constant.

## Additional Symbols

| | |
|---|---|
| $f_\alpha$, $f_\beta$ | The frequency at which the magnitude of the parameter indicated by the subscript is 0.707 of the low frequency value. |
| $f_1$ | The frequency at which the modulus of $h_{fe}$ is equal to unity. |
| $I_{CBO}$, $I_{CEO}$ | The collector current when the collector is biased in the reverse (high resistance) direction with respect to the reference terminal and the other terminal is open circuited. |
| $V_{(BR)}$ | Breakdown voltage. |
| $V_{(BR)CBO}$, $V_{(BR)CEO}$ | The breakdown voltage between the terminal indicated by the first subscript when it is biased in the reverse (high resistance) direction with respect to the reference terminal and the other terminal is short circuited. |
| $V_{CE(\text{sat})}$ | Collector-to-emitter saturation voltage. |
| $V_{CE(\text{knee})}$ | Collector knee voltage. |
| $P_{\text{tot}}$ | Total power dissipated within a device. |
| $T_{\text{amb}}$ | Ambient temperature. |
| $T_j$ | Junction temperature. |
| $r_e, r_b, r_c$, $c_e, c_c, \alpha, \beta$ | Components of the common base small-signal T equivalent circuit. |
| $r_{bb}, r_{be}, c_{be}$, $r_{bc}, c_{be}, r_{ce}$, $r_{bc}, g_m$ | Components of the small signal hybrid-equivalent circuit. |

$g_m$ is also used as the mutual conductance of a thermionic valve.
$r_a$ the anode resistance of a thermionic valve.
$\mu$ the amplification factor of a valve.

# Bibliography


1. ZIMMERMAN, H.J. and MASON, S.J., *Electronic Circuit Theory*, Wiley, New York, 1959.
2. LANGMUIR, I., *Phys. Rev.* **2,** 1913.
3. VALLEY, G.E. and WALLMAN, H., *Vacuum Tube Amplifiers*, McGraw-Hill, New York, 1948.
4. MILLER, J.M., *Sci. Pap. U.S. Bur. Stand.* No. 351, 1919.
5. SHOCKLEY, W., *Bell Syst. tech. J.* **28,** July 1949.
6. SHOCKLEY, W., *Holes and Electrons in Semiconductors*, Van Nostrand, New York, 1950.
7. JAMES, J.R. and BRADLEY, D.J., *Electron. Technol.* **38,** March 1961.
8. EBERS, J.J. and MOLL, J.L., *Proc. Inst. Radio Engrs*, **42,** New York, Dec. 1954.
9. RYDER-SMITH, S.C., *Electron. Technol.* **38,** Oct. 1961.
10. *Reference Manual of Transistor Circuits*, Mullard, London, 1960.
11. CHANDI, S.K., *Trans. Inst. Radio Engrs*, C.T. **4,** New York, Sept. 1957.
12. SHEA, R.F., *Transistor Circuit Engineering*, Wiley, New York, 1958.
13. BODE, H.W., *Network Analysis and Feedback Amplifier Design*, Van Nostrand, New York, 1945.
14. TERMAN, F.E., *Radio Engineering*, McGraw-Hill, New York, 1951.
15. HAFLER, D. and KEROES, H.I., *Audio Engng.* **35,** Nov. 1951.
16. STURLEY, K.R., *Radio Receiver Design*, Chapman & Hall, London, 1947.
17. LANGFORD-SMITH, F., *Radio Designers Handbook*, Iliffe, London, 1953.
18. JOYCE, M.V. and CLARKE, K.K., *Transistor Circuit Analysis*, Addison-Wesley, New York, 1961.
19. WALSTON, J.H. and MILLER, J.R., *Transistor Circuit Design*, McGraw-Hill, New York, 1963.
20. KORN, G.A. and KORNE, T.M., *Electronic Analog Computors*, McGraw-Hill, New York, 1952.
21. WASS, C.A. and GARNER, K.C., *Introduction to Electronic Analogue Computers*, Pergamon, London, 1964.
22. PAUL, R.J., *Fundamental Analogue Techniques*, Blackie, London, 1964.
23. LYNCH, W.A., *Proc. Inst. Radio Engrs*, **39,** New York, Sept. 1951.
24. BENSON, F.A., *Electron. Engng*, **24,** Sept. 1952.
25. COHEN, E. and JENKINS, R.O., *Proc. Instn elect. Engrs*, B, **107,** May 1960.
26. WALKER, D.E., *Electron. Engng.* **34,** June 1962.

27. HULL, A.W., *Proc. Inst. Radio Engrs*, N.Y. New York, 1918.
28. BRUNETTI, C., *Proc. Inst. Radio Engrs*, **27**, New York, 1929.
29. SOMMERS, H.S., *Proc. Inst. Radio Engrs*, **47**, New York, July 1959.
30. THOMAS, H.A., *The Theory and Design of Valve Oscillators*, Chapman & Hall, London, 1951.
31. SANDEMAN, E.K., *Radio Engineering*, Chapman & Hall, London, 1947.
32. MCCANN, M.R., *The Tunnel Diode as an Oscillator*, S.T.C. App. Report, London, 1961.
33. VAN DER POL, B., *Phil. Mag.* **2**, 1926.
34. ABRAHAM, H. and BLOCH, E., *Ann. der Physik*, **12**, 1919.
35. MILLMAN, J. and TAUB, H., *Pulse and Digital Circuits*, McGraw-Hill, New York, 1956.
36. ECCLES, W.H. and JORDAN, F.W., *Radio Rev.* **1**, London, 1919.
37. CHANCE, B., *Waveforms*, McGraw-Hill, New York, 1948.
38. NEETESON, P.A., *Junction Transistors in Pulse Circuits*, Philips Tech. Lib., Eindhoven, 1959.
39. BEAUFOY, R., *J. Instn elect. Engrs*, May 1959.
40. SCHMITT, O.H., *J. Sci. Instrum.* **15**, Jan. 1938.
41. WILLIAMS, F.C. and MOODY, M.F., *J. Instn elect. Engrs*, IIIA, **7**, 1946.
42. DUMMER, G.W., *Fixed Resistors*, Pitman, London, 1956.
43. DUMMER, G.W., *Fixed Capacitors*, Pitman, London, 1956.
44. *The Use of Electronic Valves*, Brit. Stand. Code CP1005, London, 1954.
45. PEARLSTON, C.B., *Trans. Inst. Radio Engrs*, R.F. **14**, New York, Oct. 1962.
46. JAEGER, J.C., *An introduction to the Laplace Transformation with engineering applications*, Methuen, London, 1949.
47. VAN VALKENBURG, M.E., *Introduction to Modern Network Synthesis*, Wiley, New York, 1959.
48. WEINBERG, L., *Network Analysis and Synthesis*, McGraw-Hill, New York, 1962.

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